

Device Modeling

Dr. Robb Johnson, Director of Technology



Why Model?

- **State-of-the-art technologies often do not have state-of-the-art models**
- **Competitive edge over other companies using the same foundry**
- **Better understanding of device characteristics and their strengths and weaknesses**

Modeling Challenges

- Accurate models over temperature and bias up to 100 GHz
- Devices with f_T up to 200 GHz require good calibration and de-embedding
- Standard models in simulators are optimized for silicon-based devices
- Corner models are needed to accommodate process variations

Hardware Platform



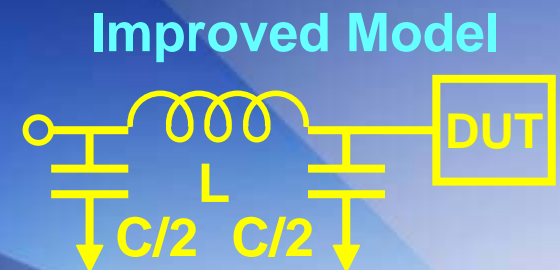
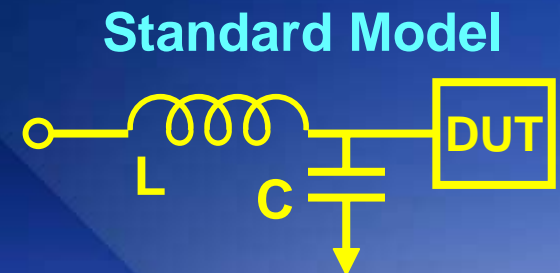
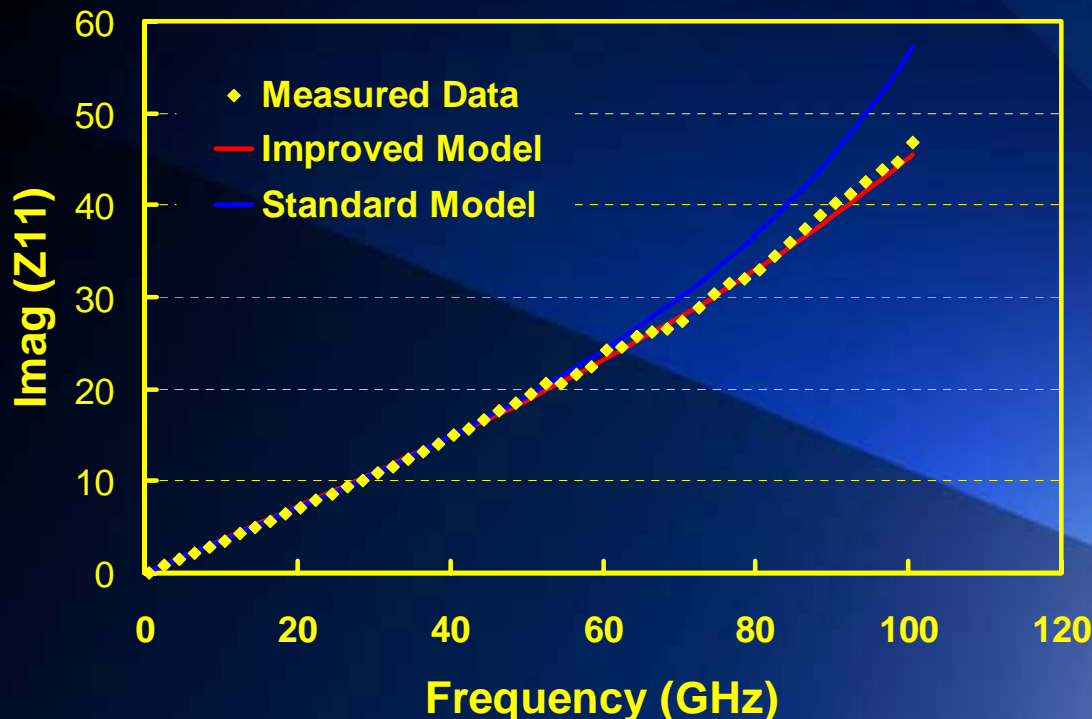
- **RF source**
 - Agilent 8510C vector network analyzer
 - Agilent 8510XF millimeter-wave controller (50 MHz – 110 GHz)
- **DC source**
 - Agilent 4142B modular DC source / monitor
- **Probe station**
 - Karl Suss PA200 automated prober
 - Trio-Tech thermal chuck (–40°C – 200°C)

Software Platform

- **Agilent IC-CAP**
 - Instrument controller for measurements
 - Tied into Spectre and ADS for simulation
- **Cadence CIC (custom IC) design tools**
 - Analog design environment – Spectre
 - RF design environment – Agilent EEsof RFDE
- **Agilent ADS**
- **IDS DataPower**
 - PCM and circuit data analysis

Parasitic De-Embedding

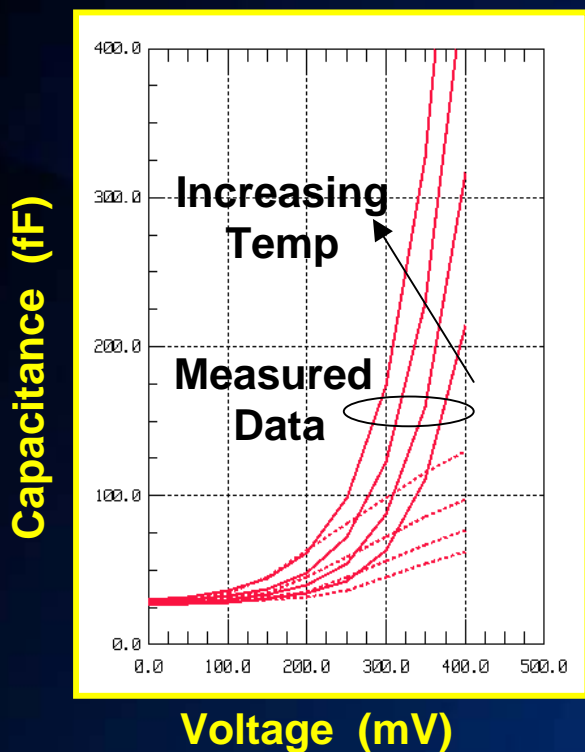
- Pad parasitics must be de-embedded from device measurements
- Simple LC model of pads not accurate at $f > 50$ GHz
- Distributed CLC network more accurate up to 100 GHz



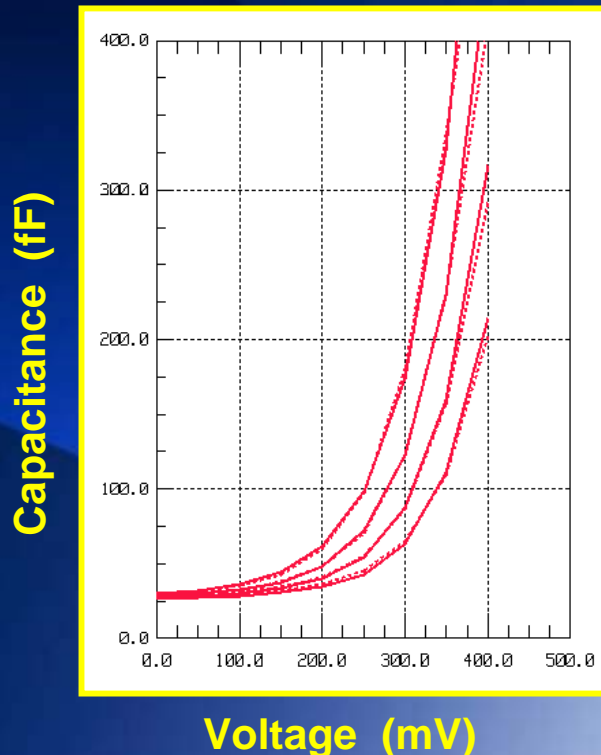
Overcoming Model Deficiencies

- Standard model does not adequately model capacitance as a function of voltage and temperature
- Custom model to improve model

Standard Model

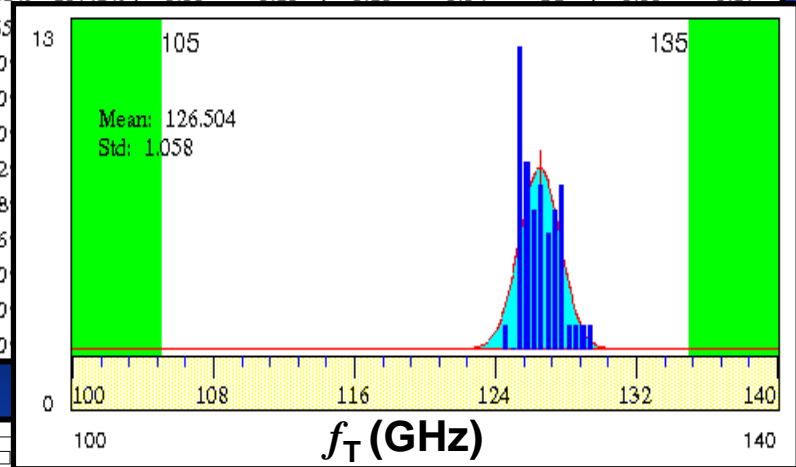


Improved Model

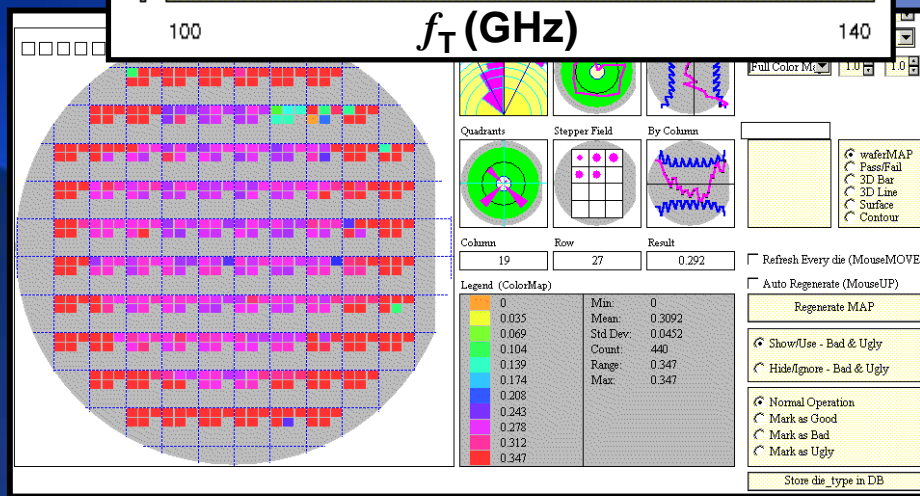


Corner Modeling

Parameter			Yield Analysis			Actual Yield Loss			Prod. Limits		Mean	Std Dev	data Pnts	data Min	data Max	
No.	Units	Description	Cpk	Mean	+/-3 Sigma	Yield Loss	Loss	Adjst	Cumult	Lower						Upper
37.00	0.00	1x20_Beta	3.91		+		0%	0.00%	0.00%	45.00	75.00	61.40	1.16	31	58.94	62.91
38.00	0.00	1x20_Vbe	9.59		+		0%	0.00%	0.00%	0.71	0.87	0.81	0.00	31	0.81	0.81
44.00	0.00	1x20_Vce_Offset	0.06				35.48%	35.48%	35.48%	0.06	0.10	0.10	0.04	31	0.00	0.17
45.00	0.00	1x20_BVceo	0.13				25.81%	16.65%								
46.00	0.00	1x20_BVebo	99.00				-	0.00%								
47.00	0.00	1x20_BVcbo	99.00				-	0.00%								
58.00	0.00	1x10_Beta	4.39		+		0%	0.00%								
59.00	0.00	1x10_Vbe	-0.05				16.13%	7.72%								
65.00	0.00	1x10_Vce_Offset	0.16				16.13%	6.48%								
66.00	0.00	1x10_BVceo	0.19				9.68%	3.26%								
67.00	0.00	1x10_BVebo	99.00				-	0.00%								
68.00	0.00	1x10_BVcbo	99.00				-	0.00%								
79.00	0.00	1x7_Beta	4.84		+		0%	0.00%								



- Create models based on physical measurements (e.g. sheet resistance) rather than arbitrarily fitting parameters
- Use PCM data to determine process corners and create device corner models



Conclusions

- Parasitic de-embedding of pads can be achieved with distributed model
- Model limitations can be overcome with custom model implementation
- Corner models can be achieved with synergy between process control monitor data and model parameters

Presenter Biographies (con't.)

Dr. Robb Johnson, Director of Technology. Dr. Robb Johnson comes to Inphi from IBM Microelectronics, where he managed the SiGe Technology Development Group in Burlington, Vermont. While with IBM, Dr. Johnson was instrumental in the development of their SiGe BiCMOS processes. Throughout his career, Dr. Johnson has worked on the design, fabrication, characterization, and modeling of transistors and passive elements at radio frequencies and has implemented them in basic RF building blocks. Dr. Johnson has authored or co-authored more than 25 papers and conference proceedings in the fields of silicon-on-sapphire MOSFETs and SiGe HBTs. He received his B.S., M.S., and Ph.D. in electrical engineering from the University of California, San Diego.

