

A Low Cost Digital Eye Analyzer

- 1. Abstract:** For design, debugging and production, digital signals are analyzed using a Digital Eye Analyzer (DEA). A DEA is a digital sampling scope which can plot and analyze the eye diagram of the digital signal. Various key parameters for digital signals, such as extinction ratio, optical average power, signal to noise ratio, rise/fall time, jitter, eye mask compliance, etc. are specified by the pertinent standard and should be guaranteed and maintained for reliable operation. DEAs are used to measure these parameters to validate the compliance. Traditional DEAs are expensive and bulky, which limits their use. In this paper, we will present a low-cost DEA that can benefit both field and production testing as well as a lab bench-top tester. The proposed low-cost DEAs are able to cover data rates as high as 12.5 Gb/s and can be built for under \$1000.
- 2. Application Space:** Analog signals, e.g. VGA signals, are getting replaced with digital signals, e.g. HDMI and display port. Parallel interfaces, e.g. PCI, are getting replaced with serial interfaces, e.g. PCIe. Most of these standards have serial digital signals of 1-11 Gb/s. Table 2.1 names a few of the popular standards with respective data rates.

Standard	Serial per lane Data Rate
Video Broadcast HD-SDI	1.485/2.97 Gb/s
HDMI	3.4 Gb/s
Display Port	1.62/2.7 Gb/s
USB 3.0	4.8 Gb/s
PCIe	2.5/5.0/8 Gb/s
SATA	1.5/3/6 Gb/s
Infiniband	2.5/5.0/10 Gb/s
Fiber-channel	2.125/4.25/8.5 Gb/s
XAUI, 2X HAU1	3.125/6.25 Gb/s
Ethernet	10.3125 Gb/s
SONET OC48/OC192	2.48832/9.95328 Gb/s

Table 2.1

DEAs are the best instruments for design, final test in production and troubleshooting in the field. These DEAs are commonly used in design labs where prototype components or systems are designed for the first time. Though DEAs are currently being used for production testing, ramping volume and falling product prices makes them unviable day-by-day for production test. Due to the prohibitive cost and size, traditional DEAs cannot be used for field testing.

2.1: Production Tester: For components and systems, the low-cost DEA can be used for production test. With near wire-speed data capture and processing, the throughput can be increased significantly over a traditional rack-and-stack tester using a high-end scope and computer, which is limited by the data transfer between scope and computer. Due to significantly lower cost, the set-up can be duplicated as per production need, and the volume is not limited by expensive Automatic Test Equipment (ATE) or rack-and-stack equipment.

2.2: Field Tester: Portability is a prime concern for field test equipment. Traditional DEAs are based on sampler hybrid modules, which are made with discrete microwave components. Due to the nature of sub-assembly, they are housed in bulky modules (typical size ~28 mm X 24 mm X 12 mm). They require several power supplies for proper biasing of circuits (typically 4 supplies, two positive and two negative). With these limitations, a traditional DEA is also bulky, expensive and non-portable.

The proposed DEA is based on a track and hold amplifier, which is a microchip packaged in 4 mm X 4 mm X 1 mm package. This only requires one power supply. Because it is a microchip, the cost is also an order of magnitude lower. With these advantages, now field test equipment can have eye capturing capability.

2.3: Inexpensive Bench Top Tester: Due to the explosion of SerDes-based serial communication protocols, hardware engineers cannot use traditional logic analyzers and low-frequency, real-time scopes. Though high-end DEAs will co-exist for precision characterization, inexpensive low-cost bench-top testers can be utilized by board designers for troubleshooting purposes. Due to its low cost, designers can have dedicated testers.

3. Usage Model: Some systems are serial-in-serial-out while others either generate a serial signal or receive a serial signal. Based on this usage, we classify two system-level usage models: serial-in-serial-out and parallel-serial systems.

3.1: Serial-in-serial-out Systems: For serial-in-serial-out systems, typically a Bit Error Rate Tester (BERT) is used along with a DEA scope as shown in Fig 3.1.1. The Bit Error Rate Tester generates a pattern and also provides serial clock along with a pattern trigger. The pattern trigger provides a pulse signal, which indicates the start of a pattern. The Device Under Test (DUT) takes the data from the BERT's Pattern Generator, and the output of the DUT is fed into the BERT. While the BERT tests the error rate, other analog properties of the DUT's output are best tested with a DEA, which can measure jitter, rise/fall time, eye mask, etc. If there is any issue with DUT, the troubleshooting is performed by the scope. Most BERTs do not provide enough insight to troubleshoot or thoroughly characterize the DUT.

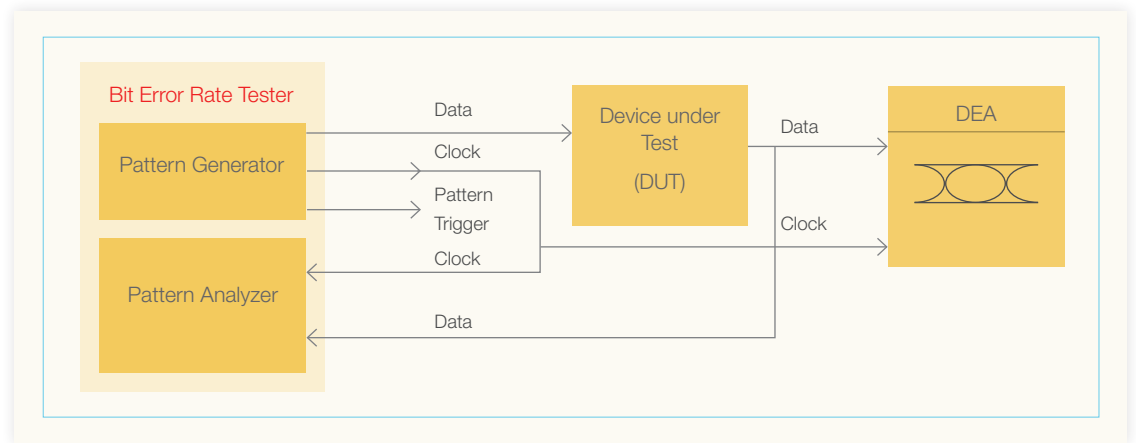


Figure 3.1.1: Serial-in-serial-out DUT testing

Fig 3.1.2 shows one example of a simple serial-in-serial-out system test. The serial signal could go into a cable driver which conditions the signal as per the standard. Then the signal runs over applicable transmission media, e.g. co-axial cable. The signal is received at the other end by an equalizer. The combination of cable driver, coax cable and the cable equalizer is considered DUT in this application.

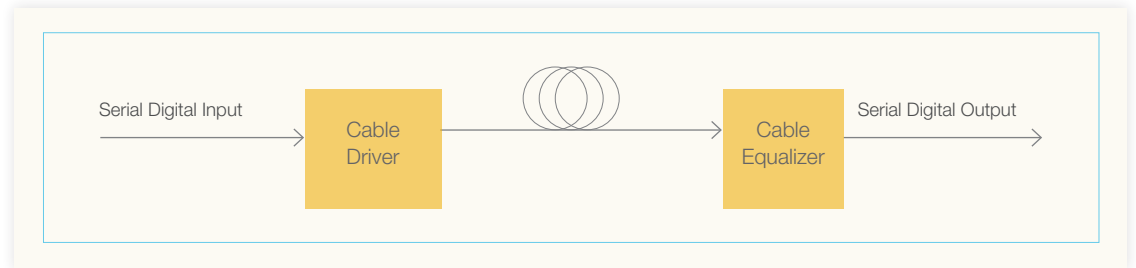


Figure 3.1.2: Example of Serial-in-serial-out DUT

3.2: Parallel-Serial Systems: Certain systems, e.g. a video color bar pattern generator, produce a serial signal with no serial input. In some of these systems, a serial clock is not available. The unavailability of the serial clock makes it difficult to test these systems. Triggering to serial data could produce misleading results and is not recommended. There are two options possible to analyze these systems.

3.2.1: Reference Parallel Clock: If a parallel clock is available in the parallel-serial system, it can be used for triggering DEA. Fig 3.2.1.1 shows the configuration.

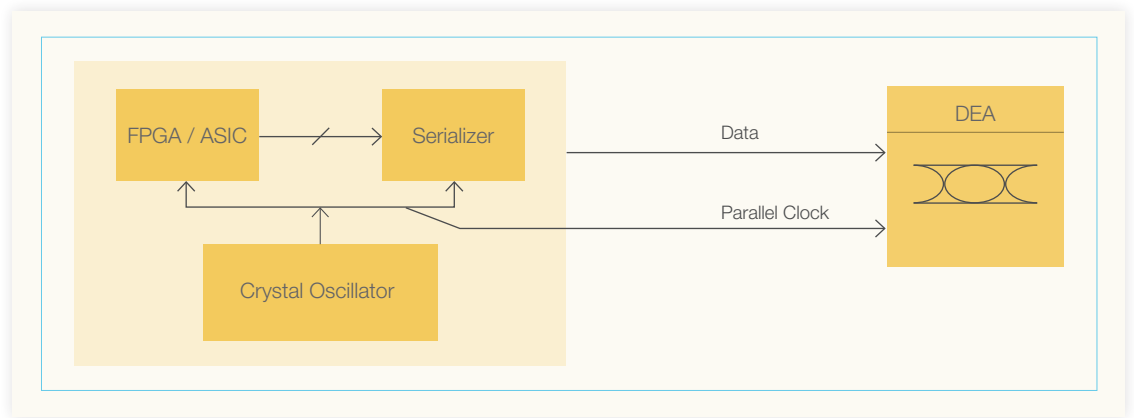


Fig 3.2.1.1. Triggering DEA with parallel clock

3.2.2: Clock Recovery Unit: A clock recovery unit is required to generate a serial clock, which can be used to trigger the error detector and scope for eye analysis. Fig 3.2.2.1 shows the configuration. The passive splitter and clock recovery unit can be included in the DEA.

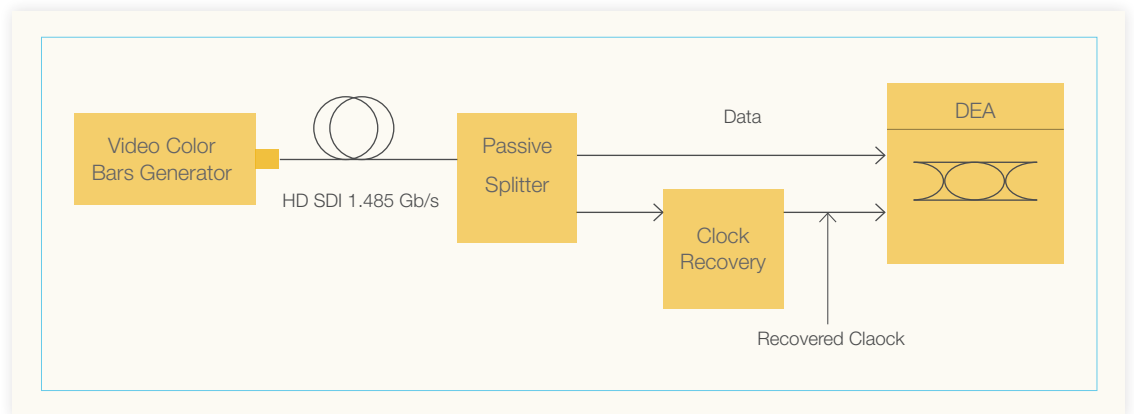


Fig 3.2.2.1. Triggering DEA with recovered clock

4. Basics of Digital Eye Analyzer: A digital eye analyzer is a digital sampling oscilloscope, e.g. Agilent 86100, Tek DSA8200. Using a digital sampling scope, the eye analysis can be performed irrespective of the sampling rate. Most digital sampling scopes sample the incoming eye at less than 10 MHz while the serial data rate can be as high as 40 Gb/s. Parameters such as jitter, rise/fall time, amplitude, extinction ratio, etc. can be measured accurately without sampling at serial clock speed. A high level block diagram of an oscilloscope is shown in Fig 4.1. There are three key building blocks: A voltage sampler, timing generator and software for display.

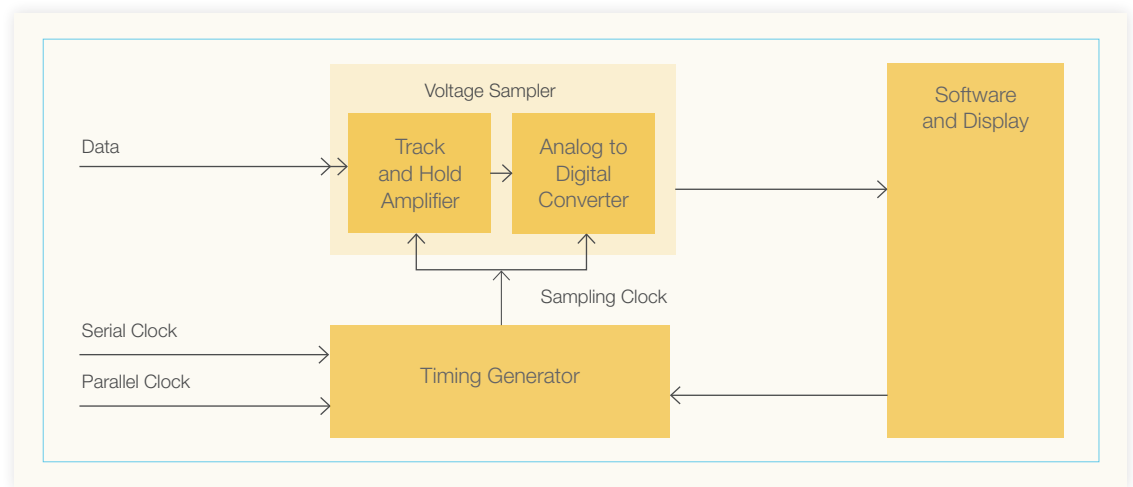


Fig 4.1. Key Building Blocks of a Digital Communication Analyzer

4.1: Voltage Sampler: A circuit that can digitize the input signal is the most crucial building block. For high bandwidth application, typically this block is implemented in two components.

4.1.1: Track and Hold Amplifier (THA): The front end bandwidth of the track and hold circuit determines the bandwidth of the communication analyzer. Inphi has two THA offerings, 1321TH and 1821TH. The 1321TH is a 13 GHz front end bandwidth track and hold, which is packaged in an inexpensive plastic QFN package. The 1821TH has 18 GHz bandwidth and is packaged in a high-performance ceramic BGA package for applications that require higher bandwidth.

4.1.2: Analog to Digital Converter (ADC): Once signal is sampled with track and hold, a commodity ADC with 50-200 MHz analog front end bandwidth could be used to digitize the THA output. 8-16 Bit of full-scale resolution is sufficient in most cases.

4.2: Timing Generator: A timing generator takes the serial or parallel clock and generates a sampling clock. If the input clock is a serial clock, then clock dividers are used to bring the clock down to the rate that is compatible with the ADC choice. Not only does the clock have to be brought down to lower rates, it has to be delayed in precision steps to sample the incoming digital signal at various points over one unit interval (UI) so the resulting data eye can be plotted on the screen. The delay generation in high-end DEAs is proprietary to the scope vendors and a highly guarded secret by them. There are simple methods for timing generation using off-the-shelf components shown in Fig 5.2.1.

4.3: Software and Display: The software controls the timing generator and captures data from the voltage sampler. With a known relationship between sampling time and corresponding captured data, it can plot the eye and measure parameters, such as jitter, amplitude, rise/fall time etc.

5. Detailed DEA Architecture:

5.1: Voltage Sampler: The voltage sampling block is divided into three sections. Fig 5.1.1 shows the proposed architecture.

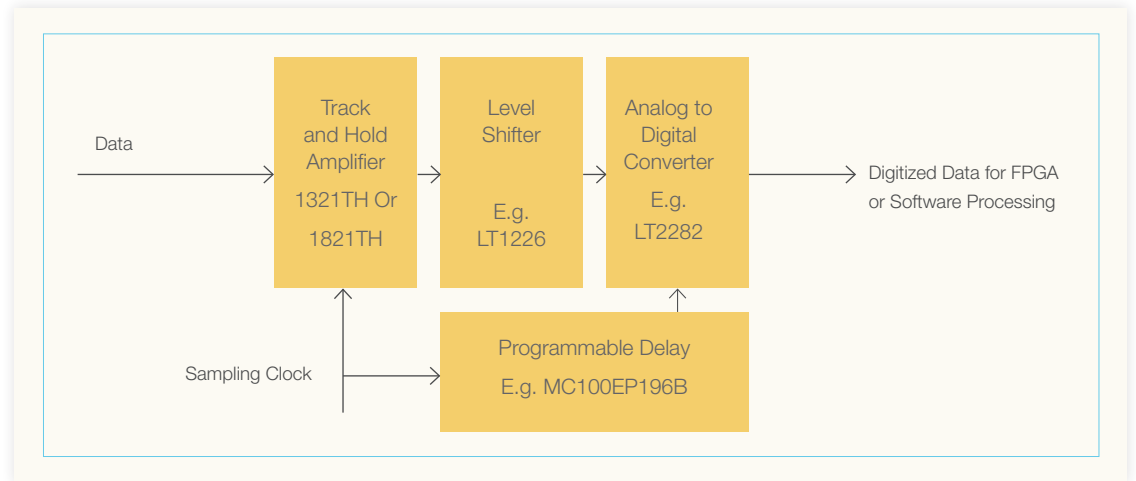


Fig 5.1.1 Details of Voltage Sampler

5.1.1: Track and Hold amplifier: There are two choices for the sample and hold. The 1321TH can be used if the data rates are under 7 Gb/s. For data rates up to 12.5 Gb/s, the 1821TH is recommended. The 1321TH is packaged in a low-cost plastic package, which provides cost-effective solutions, whereas the 1821TH is a performance optimized ceramic BGA package. Both the 1321TH and 1821TH require only one -5.2V supply with 265 mA type current. Input can be AC coupled, if needed. There are on-chip 50 ohm terminations to ground. It should be noted that the input voltage should not exceed +/-0.5 V. AC coupling will provide protection against accidental shortage to higher voltage levels. The value of the AC coupling capacitor should be chosen according to the data rate and the standard. For example, for an SMPTE 270 Mb/s SDI application, 4.7uF will be an ideal capacitor, and for 10 Gb/s OC192, 100 nF will be an ideal capacitor. Output should be DC Coupled. The minimum sampling rate should be kept above 20 MHz. The maximum sampling rate can be as high as 2 Gb/s, though it is recommended to keep it under 200 MHz to keep the cost of the level shifter and ADC low.

5.1.2: Voltage Level Shifter: Both the 1321TH and 1821TH operate with input signal levels whose common mode potential is within +/-0.5V. The common mode of the output is -0.5V. Most ADCs accept signals with 1V-3.3V common mode voltage. A voltage level translator is needed to couple the THA and ADC. Operational amplifier-based level translators can be used since the signal generated by the THA is composed of lower frequencies (in the range of 20-200 MHz). An example of Op-amp that can be used for this purpose is a Linear Technology Op-amp LT1226.

5.1.3: ADC: A common off-the-shelf ADC with input bandwidth of 20 MHz to 200 MHz can be used depending on the sampling clock. The bandwidth should be similar or higher than the sampling clock frequency. One example of the ADC that can be used is the Linear Technology LT2282. The delay between clocking of THA and ADC is critical. The delay has to be optimized based on the clock to output delay of the track and hold, level shifter and front-end delay of the ADC. It is very difficult to anticipate the optimum delay, so it is recommended that a programmable delay (e.g. ONsemi MC100EP196B) in the path of the ADC clock be provisioned.

5.2: Timing Generator: The optimal sampling frequency is recommended to be in the range of 20-200 MHz, though it can be as high as 2 GHz. If the input serial or parallel clock is more than 200 MHz, then it can be divided down to get in the range of 20-200 MHz. The divided clock could be selected using a selector chip. Fig 5.2.1 shows the architecture.

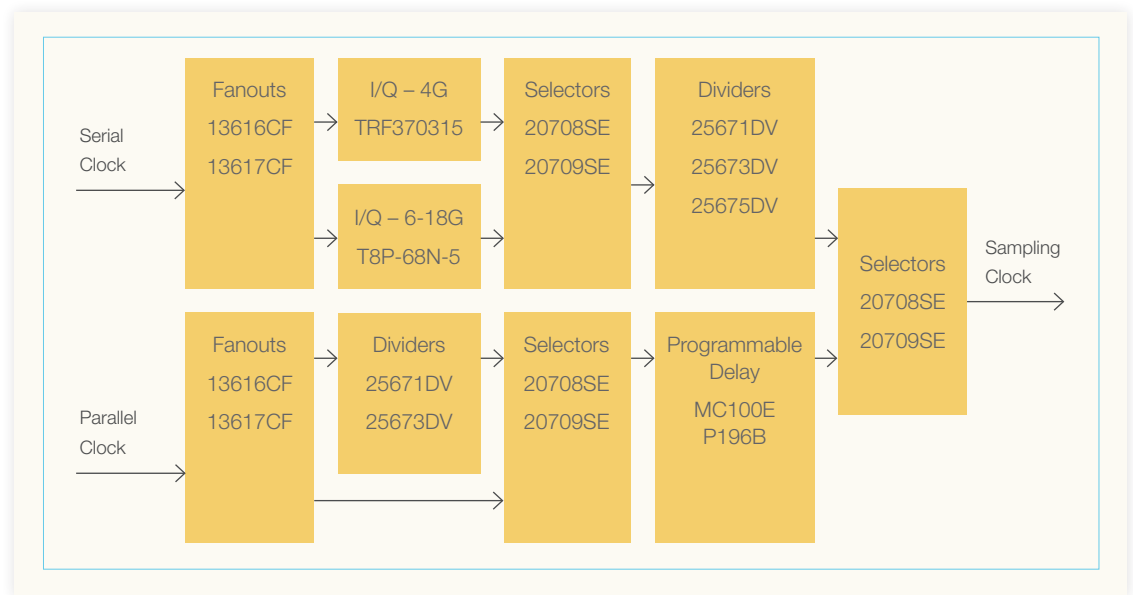


Fig 5.2.1 Timing Generator

5.2.1: Serial Clock: An I/Q modulator can be used as a block which shifts the clock in small steps. Typically, the I/Q modulators come in frequency bands. For example, TRF370315 can be operated between 400 MHz to 4 GHz. I/Q modulators can be used as the phase shifter or programmable delay¹. To cover broader frequency range, multiple I/Q modulators covering various ranges can be used in parallel. A clock fan-out circuit, e.g. 13617CF, and a selector circuit 20709SE can be used to connect multiple band I/Q modulators as shown in Fig 5.2.1. For high-end performance, the delay steps can be calibrated during production. For operation over temperature, either the delay block is kept at calibration temperature using a thermo-electric-cooler or other temperature stabilization methods, or temperature dependent calibration can be done and a look-up table could be used during operation. Real-time calibration is also possible, but is beyond the scope of this white paper.

5.2.2: Parallel Clock: Programmable delay with analog fine control, e.g. ONsemi MC100EP196B, can be used as a timing generator. MP100EP196B has about 8000 ps of delay in 10 ps steps. To bridge the gap between 10 ps of digital steps, analog delay can be used. The generous 50 ps of analog delay is more than sufficient to bridge the gap. The 8000 ps can capture eyes for data rates as low as 125 Mb/s. This method does not pose any limit on higher data rates. The calibration can be done in the same manner explained in section 5.2.1.

6. Capturing the Eye: The incoming digital signal is scanned for one UI (bit period). Depending on what resolution is required, 100 to 256 delay settings within one bit period are more than sufficient for the majority of applications. For finer resolution, the DAC used for delay control could be increased in bit resolution. For each delay setting, 100-1000 samples are considered more than sufficient for most eye analysis. However, there is no limit on how many samples can be collected for each delay setting.

The eye can be scaled and shifted vertically and horizontally to maximize the use of the display, once the one full bit period eye is captured. Various parameters, such as rise/fall time, eye mask margin, etc. now can be measured once the eye is displayed on the screen.

6.1: Demo Set-up and Measurement Results: Fig 6.1 shows the block diagram of the lab demo set-up.

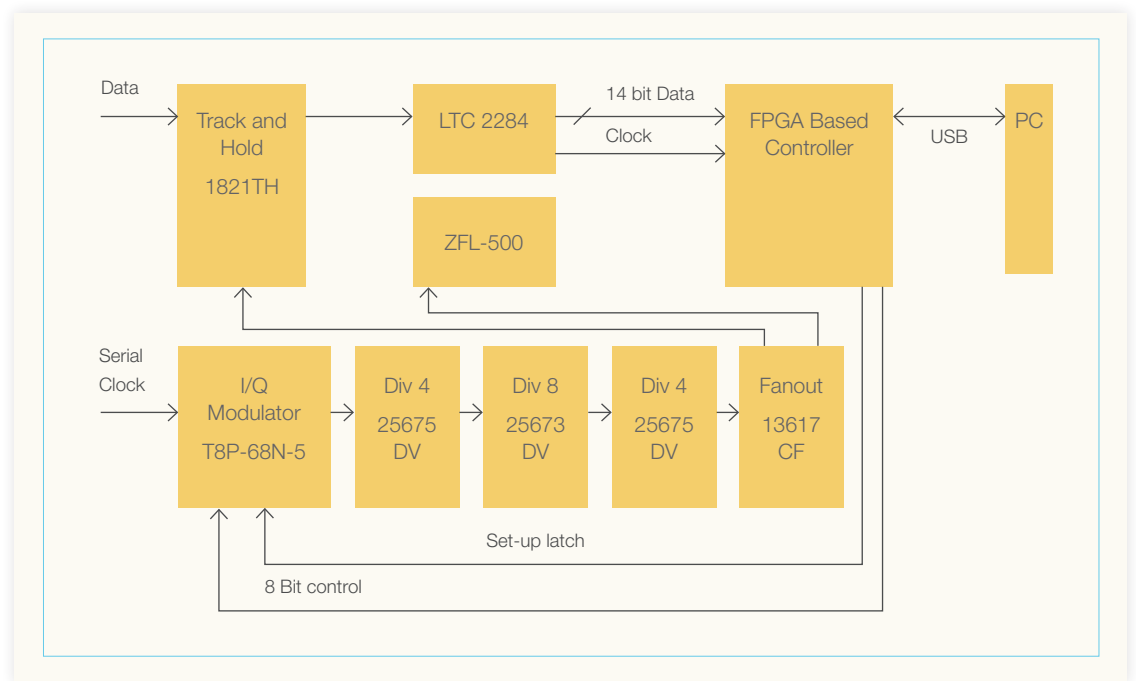


Fig 6.1 Lab demo set-up block diagram

Both data and serial clock was generated by SyntheSys Research's BERTScope. A 7.5 GHz filter Picosecond Pulse Labs 5933-110-7.48G was used as per OC192 standard to filter the data signal at the track and hold input. 1821TH was used as the track and hold amplifier. For timing generation, GT-microwave T8P-68N-5 was used as the I/Q modulator. Two divide-by-four frequency dividers (25675DV) and one divide-by-eight frequency divider (25673DV) were used to divide a 10 GHz clock down to 78 MHz. A Fanout buffer 13617CF was used for fanning out the clock. An amplifier (Mini circuit ZFL-500) was used to generate a TTL compatible clock signal to trigger LTC2284 ADC. An Altera FPGA was used to capture the data. The captured data is transferred to the PC. Fig 6.2 shows the lab set-up.

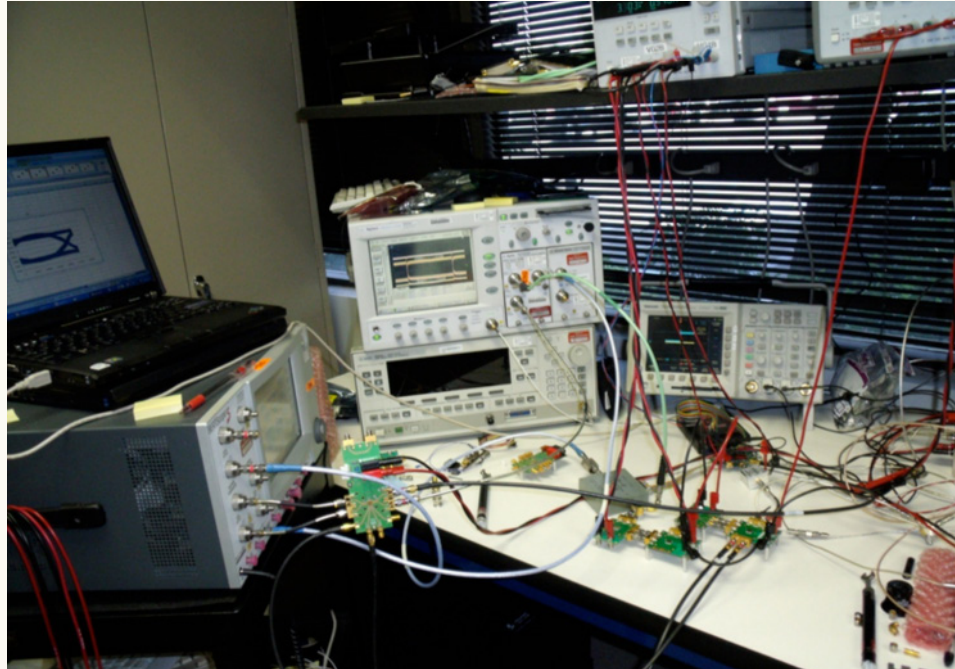


Fig 6.2 Demo Set-up

Fig 6.3 compares the captured eye to the eye captured by 70GHz Agilent scope.

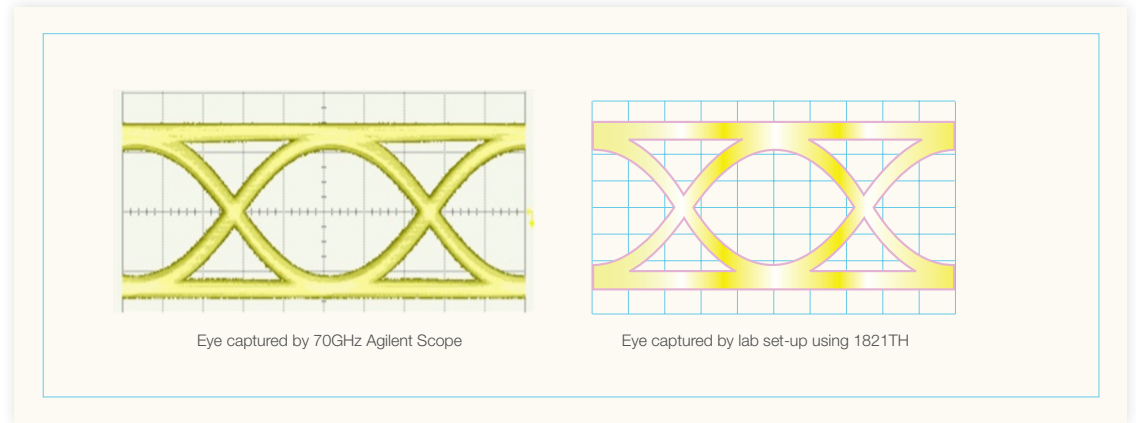


Fig 6.3 Comparison of the measured eye with 70Ghz Agilent scope and the demo set-up using 1821TH.

- 7. Conclusion:** In this white paper, we discussed how to assemble a Digital Eye Analyzer using one Track and Hold amplifier and other commodity components. The demo set-up captured the eye which shows no compromise in signal integrity with respect to high-end scopes. For higher throughput, the captured data can directly be analyzed in real time which is not possible with off-the-shelf high-end scopes. This provides near wire speed testing which increases the through-put by order of magnitude.

References:

1. http://www.gtmicrowave.com/Phase_Shifters_Vector_Modulator.pdf



Inphi Corporation
112 S. Lakeview Canyon Rd.
Suite 100
Westlake Village, CA 91362
Phone: (805) 719-2300

Inphi Corporation
3945 Freedom Circle
Suite 1100
Santa Clara, CA 95054
Phone: (408) 217-7300

Web: www.inphi.com