

InP HBT Ring Oscillator with 2.0ps/stage Gate Delay

N.K. Srivastava, G.Raghavan, R.Thiagarajah, M.G.Case, E.Arnold, C.W.Pobanz, S.O.Nielsen, J.C. Yen, R.A.Johnson

Inphi Corporation.

2393 Townsgate Road, Suite 101, Westlake Village, CA – 91361

nsrivas@inphi-corp.com

Abstract

We have demonstrated a record gate delay of 2ps/stage in a 17-stage ring oscillator fabricated in a 170GHz f_t , 150 GHz f_{max} InP HBT technology. Stable operation was achieved for both normal and higher order ring modes. We performed basic circuit time constant analysis as well as detailed computer simulations, and arrived at calculated gate delays which are in agreement with our experimental results. The approach of using stage delay from a ring oscillator as a technology speed metric can be misleading. Such an approach would predict 250 GHz circuits in this process – which is not feasible. Real circuits require fanout of two or more which can substantially increase gate delay. In our circuit, we focused on broad-banding each individual stage and reducing interconnect parasitics to achieve the above result.

INTRODUCTION

InP based HBT technology is becoming the technology of choice in a wide variety of high speed digital and mm-wave applications. The high electron velocity in InGaAs and InP compared to Silicon result in devices with an optimal combination of high speed at low power. InP HBTs offer low cost for moderate volume applications such as, the high performance segment of fiberoptic and wireless markets. InP HBT based circuits have been successfully used in critical components for OC-768 optical communication networks and beyond. Demonstrated circuits in InP include 50 Gb/s 4:1 MUX [1], 53 Gb/s 1:4 DMUX [2], and 75Gb/s divider [3] at power levels a factor of 2-3 times lower than comparable results in Silicon-Germanium.

Ring oscillators (RO) have been used as a simple method for evaluating a device technology for logic applications. There have been a number of demonstrations of gate delays less than 10ps in both Bipolar and FET logic families using the same. The most recent one by IBM [4] demonstrated a delay of 4.23ps per stage. A gate delay (T_d) of 4.7ps has been shown in AlInAs/InGaAs HBT[5] and Umeda demonstrated a 4.6ps gate delay in InAlAs/InGaAs HEMT's [6]. However, recently gate delays calculated from ring oscillators have been used to predict circuit performance at over 110 GHz in SiGe [4]. Such calculations would result in 250 GHz performance in InP based on our results – which is incorrect. Extrapolations of circuit performance based on ring oscillator results ignore

the fact that any “real” circuit has a fanout greater than one and the signals propagate in a ring oscillator at a much lower frequency than given by $(1/2 * T_d)$, reducing the extent of frequency dependent signal attenuation. Additionally a maximally dense layout, which can be easily done for a RO, is impractical for more complicated circuitry.

The paper is divided into three sections. The first section describes device/process technology; the second discusses circuit design and the third deals with measurements and hand calculations.

II. Device Technology

The circuits were fabricated using Global Communication Semiconductors 1.0 μ m InP/InGaAs HBT process [7]. The epitaxial layers were grown on 4” semi-insulating InP substrates using carbon doping for the base. The non-self-aligned mesa type HBTs were fabricated with wet etching techniques and a proprietary passivation technique to improve device reliability. The HBTs have $\beta > 30$, $BV_{CEO} > 3.5V$ and an $f_T / f_{MAX} = 170 / 150$ GHz at a collector-emitter voltage of 1.0V and collector current density of $1mA/\mu m^2$. The backend process is a fully planar process that uses a low permittivity dielectric with two levels of gold interconnects. The technology includes metal-insulator-metal thin-film capacitors and thin-film resistors passive components.

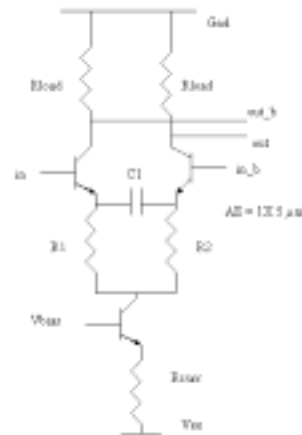


Figure 1: Circuit Diagram of single stage of Ring Oscillator shows emitter feedback and zero peaking

III. Circuit Design

The ring oscillator is designed using current mode logic (CML) inverters. It has seventeen stages and one output buffer. The circuit diagram for each stage is shown in Fig.1. $1 \times 5 \mu\text{m}^2$ and $1 \times 3 \mu\text{m}^2$ transistor sizes are used for the inverter stages and the output buffer. There is external access to the bias node instead of an onchip bias generator. This provides the flexibility to vary the current per stage and study the behavior of the ring oscillator.

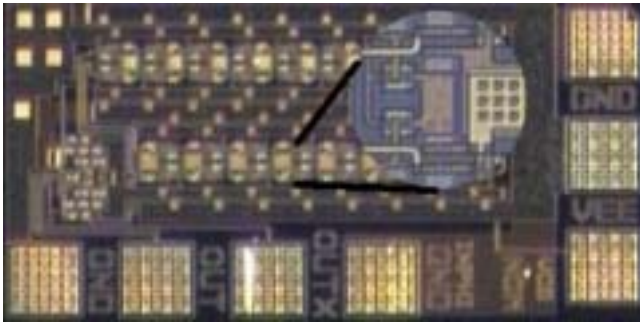


Figure. 2: Die Photograph of the ring oscillator and a single stage (inset) indicating compact layout

Emitter feedback through emitter resistors R1 and R2 is used to broadband each stage. Additionally, the capacitor C1 is used to further increase stage bandwidth through zero peaking. Care was taken during layout to minimize interconnect between stages and to tune out some of the device parasitics. In Figure 2, we show the die photo of the ring oscillator with the inset showing details of the interstage interconnect. The key to designing a fast ring oscillator lies in minimizing the time constants associated with the load resistors. However, too low a value of the load resistor would result in low gain and no oscillation. Three designs were implemented with varying values of load resistors to account for device variations. Simulations were used to determine the three resistor values for fast, nominal and slow operation. Lowest stage delay of 2 ps was obtained using a 50-ohm load resistor with 4 mA of tail current. The circuit is designed with transistors in the signal path having a V_{CE} of about 1V independent of power supply voltage. A high input impedance differential output buffer was included in the ring oscillator to drive 50-ohm loads. Minimum device sizing at low currents was used to prevent ring loading. The output buffer consists of two stages of emitter followers followed by a differential pair. It has a gain of -5dB @ 14G and -7.5dB @ 24G.

In a ring oscillator operating normally, the frequency of oscillation f_o is related to gate delay by the formula $f_o = 1/(2*n*T_d)$, where n is the number of stages and T_d is the delay/stage. Varying the tail current varies stage gain, transistor parameters and the voltage swing thus causing a variation in stage delay. Lower values of current reduce voltage swing and device delay terms resulting in lower delay/stage. Initially the ring operates in switched mode (normal mode). As the tail current is lowered further, the voltage swing decreases below the inverter switching threshold, and the ring oscillator exhibits a higher-order

“linear” oscillation around the metastable point. At lower currents, eventually the inverter gain decreases below unity and oscillations cease.

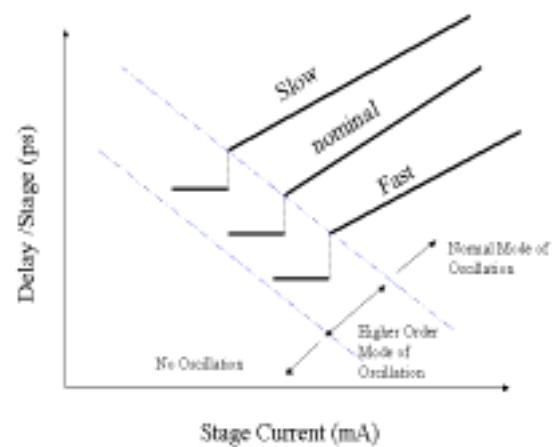


Figure. 3: Plot illustrating different regions of oscillation in the ring oscillator.

In the “linear” oscillation mode, the inverters do not switch fully and instead operate as linear amplifiers. Connected in a ring, the amplifiers will oscillate subject to the Barkhausen condition of loop gain exceeding unity and the loop output returning in-phase to the input, with extrinsic delays providing the excess phase necessary given the odd number of inversions. Contrast this with the normal, switching mode where the oscillation condition is a net inversion around the loop. Consequently, the higher-order oscillation is at approximately twice the frequency of the normal mode, with amplitude proportional to the inverters linear range. For inverters without emitter degeneration, the linear range may be too small for this higher-order mode to

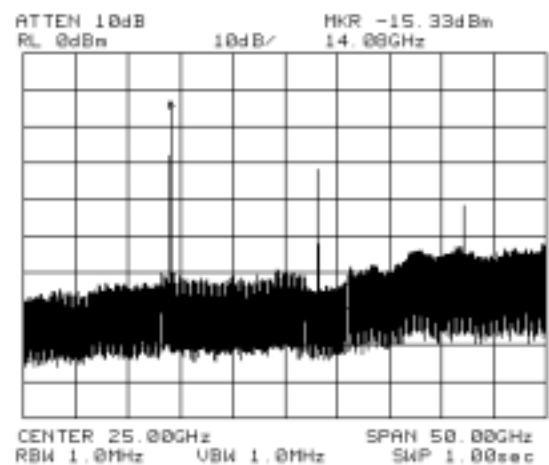


Figure. 4: Spectrum Analyzer outputs showing oscillation at 14.08GHz

be observed. As the bias currents are reduced, the output swing decreases below the switching threshold and the RO

abruptly switches from 14 GHz to 24.5 GHz. Above the switching threshold the higher-order mode cannot exist, as the linear gain decreases to zero in the fully switched logic states – and these distinct states are necessary for the normal mode of oscillation to occur. The mode transition thus provides a clear indication that the ring oscillator is operating with a complete logic-level voltage swing.

IV. Results and Discussion

The complete circuit occupies an area of 0.357mm². The measurements were done on wafer using probes at room temperature and a nominal power supply of -3.3V. The bias voltage is varied externally to vary tail current and the oscillation frequency measured using a spectrum analyzer and a digital sampling oscilloscope. The complementary output is divided by 4 and used to trigger the sampling scope for eye diagrams. Figure. 4 shows the spectrum analyzer picture of the ring output indicating proper

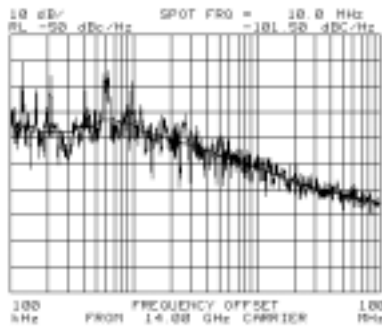
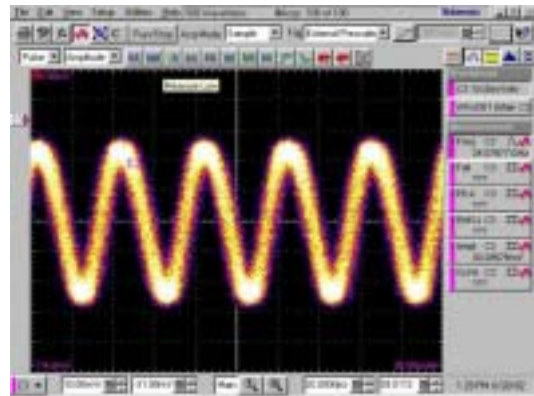
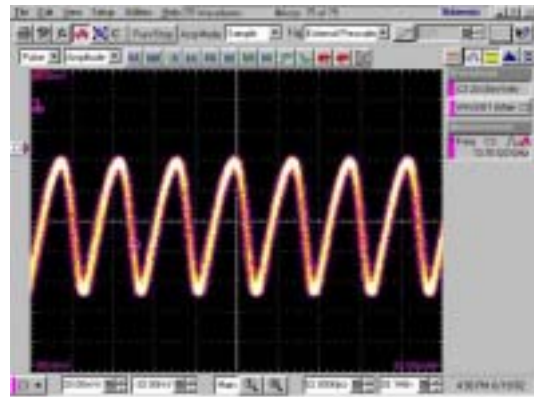


Figure.5: Phase Noise plot showing stable ring oscillator operation and phase noise of -85dBc/Hz @ 1MHz offset

oscillation. Ring oscillation in both the normal and higher order modes was found to be extremely stable. This was verified by phase noise measurements (-85 dBc/Hz @ 1MHz offset) (Figure 5) as well as in “eye diagrams” of the output (Figure 6(a)). At 13.25GHz (2.2ps stage delay) the ring amplitude is 320mV p-p (177mV p-p output amplitude). Figure 6(b) shows an “eye diagram” of a higher order mode of oscillation, it has an amplitude of 140mV p-p(58mV p-p ring amplitude) at 24.57GHz. Again, the higher order mode is also observed to be very stable.

Measurements were taken on several die across the wafer for a tail current of 4mA and the results plotted on a histogram in Fig.7. It can be concluded from the histogram that the reported gate delay is reproducible and truly representative of the designed ring oscillator. The corresponding stage delays were calculated using $f_0 = 1/(2*n*T_d)$, n=17 and plotted in Figure.8. As predicted by simulations, higher order modes were observed in measurements at low currents. Higher order mode



Figures. 6(a)(Top) and 6(b)(Bottom): Oscilloscope eye diagrams of output voltage waveforms under normal (13.76 GHz) and higher order modes (24.57 GHz) of oscillation.

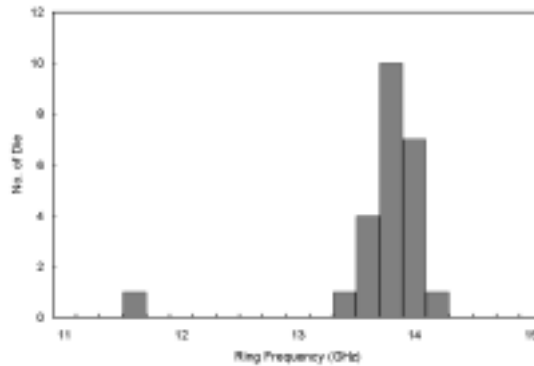


Figure. 7: Histogram shows Ring Oscillator frequency and the corresponding number of working die on wafer

oscillation frequency was measured to be 24.57GHz. These measurements were repeated on all three versions of the RO. All versions followed the trajectory shown in Figure.3 - highlighting the two regions of operation viz the normal mode and higher oscillation mode. The lowest stage delay of 2ps was obtained using a 50-ohm load resistor with 4mA of tail current in Figure.8. The voltage amplitude of the ring is also annotated on the plot.

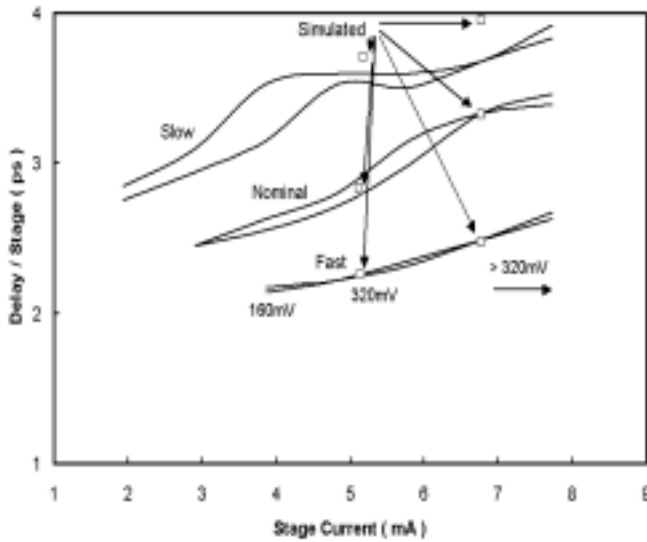


Figure.8: The plot shows RO Delay/stage as the stage current is varied, solid lines represent measured data while discrete points refer to the simulated data. The voltage amplitude of the RO are also annotated.

Table 1 shows transistors electrical characteristic for $1 \times 5 \mu\text{m}^2$ HBT devices. Using expressions for gate delay from Ref. [8],

$$(\Delta V_{\text{logic}}/I_c) * (C_{\text{cb}} + C_{\text{be, depletion}}) + R_{\text{bb}} (C_{\text{cb}} + C_{\text{be, depletion}}) + R_{\text{bb}} (\tau_b + \tau_c) (I_c / \Delta V_{\text{logic}})$$

we obtain a stage delay of

$$(100\text{mV}/4\text{mA} + 43 \text{ ohm}) * (19\text{fF}) + 43\text{ohm} * 0.42\text{ps} * (4\text{mA}/100\text{mV}) = 2.01\text{ps}$$

which matches measured results quite accurately.

Table 1. $1 \times 5 \mu\text{m}^2$ Transistor characteristics

$C_{\text{be, depletion}}$	6	fF
C_{cb}	13	fF
R_{bb}	43	Ω
$(\tau_b + \tau_c)$	0.42	ps

Based on this expression, it is evident that for high-speed circuits it is particularly important to reduce base resistance, extrinsic base collector capacitance and base-emitter depletion capacitance. In contrast to InP based HBTs, Si and SiGe based devices typically achieve much of their speed through aggressive lateral and vertical scaling of layer thicknesses and increased doping resulting in higher access resistances and capacitances. This would indicate that InP based technologies should be superior to Si based technologies for high-speed circuits.

V. Summary

This paper has demonstrated a InP HBT ring oscillator with 2ps gate delay. This is the fastest logic gate demonstration in any technology. Introducing zero peaking in each stage and having a tight layout has resulted in such low gate delay. Good correlation was obtained between simulation and measurements. Our results also correlate well with the expressions in Ref [8] which would indicate that InP HBT based digital circuits should continue to outperform Si based circuits for the highest-speed applications.

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