Process Technologies for High-Speed IC Design

Dr. Gopal Raghavan, CTO

Inphi®
Think fast.

Overview

- Technology choices
- Applications
- Reliability

Technology Choices

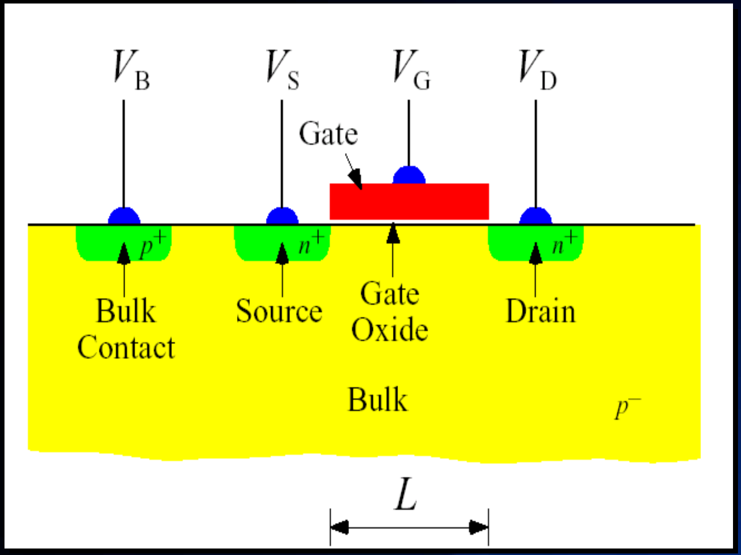
- FET technologies
  - Silicon
    - CMOS 0.13 μm gate lengths
  - Gallium arsenide (GaAs)
    - Psedomorphic high electron mobility transistor (pHEMT)
- Bipolar technologies
  - Indium phosphide (InP)
    - 1.0 μm emitter width
    - Double heterojunction bipolar transistor (DHBT)
    - Single heterojunction bipolar transistor (SHBT)
  - Silicon germanium (SiGe)
    - 0.13 μm emitter width
    - DHBT
  - Gallium arsenide (GaAs)
    - 2.0 μm emitter width
    - DHBT

Why Multiple Technologies ?

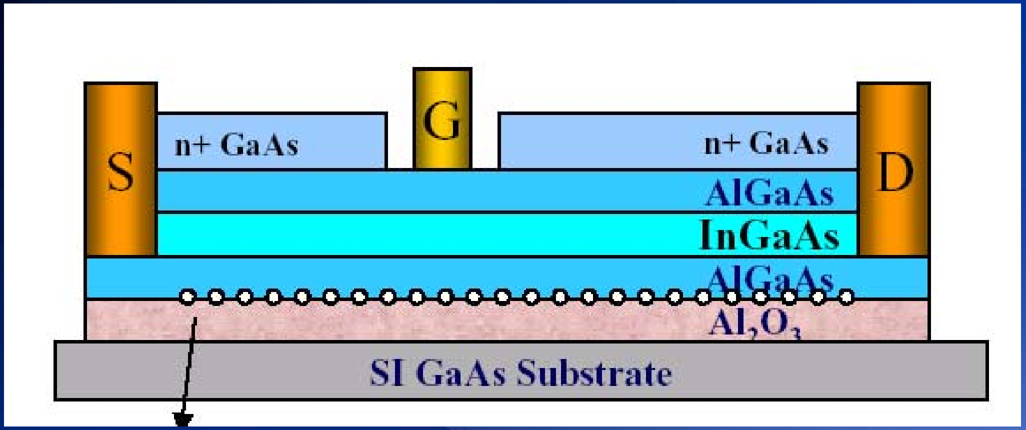
- Different applications need varying
  - Voltage swing
  - Power dissipation
  - Integration / complexity
  - Speed
  - Noise levels
  - Cost
- Many of these parameters trade off against each other
  - e.g. high voltage implies lower speed for a given structure / material
- Different technologies optimized for different applications

Inphi® Think fast.

FET Technology



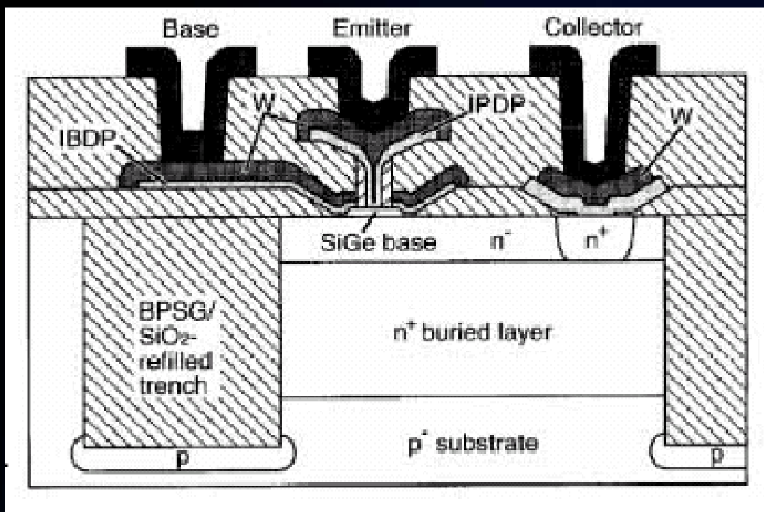
Si nMOS

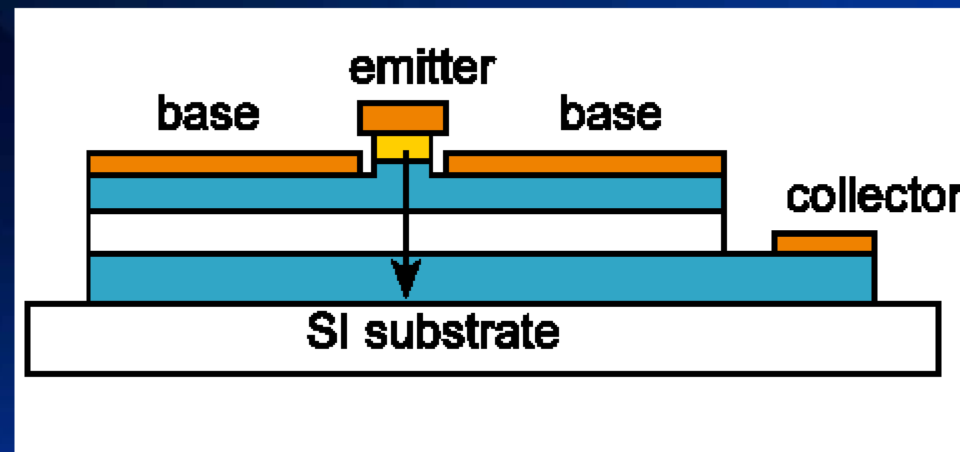


GaAs pHEMT

Inphi® Think fast.

Bipolar Technology





Low emitter, base resistance
Planar process = high yield
Passivated surfaces

Low emitter, base resistance
Low yield

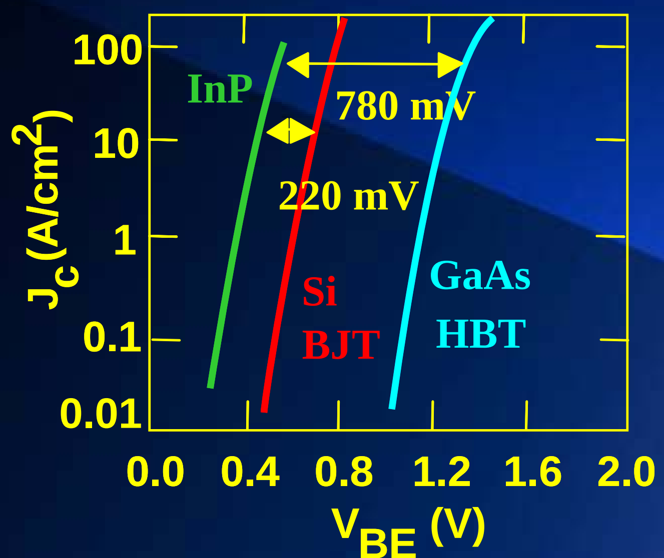
Think fast.

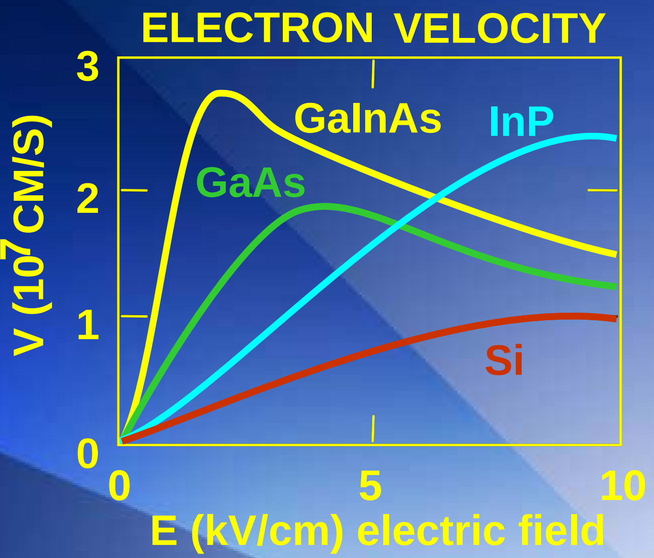
Bipolar Technology (con't.)

	Si Based	GaAs Based	GaAs Based	InP Based
SHBT		n AlGaAs p GaAs n GaAs	n InGaP p GaAs n GaAs	n AlInAs p GaInAs n GaInAs
DHBT	n Si p SiGe n Si			n InP p GaInAs n InP

InP Technology for High-Speed ICs

- Higher electron velocity in InP
  - Thicker base and collector layers compared to Si, SiGe, and GaAs
    - Lower capacitance
    - Lower current density for peak performance
    - Lower V_{be}
    - Better breakdown





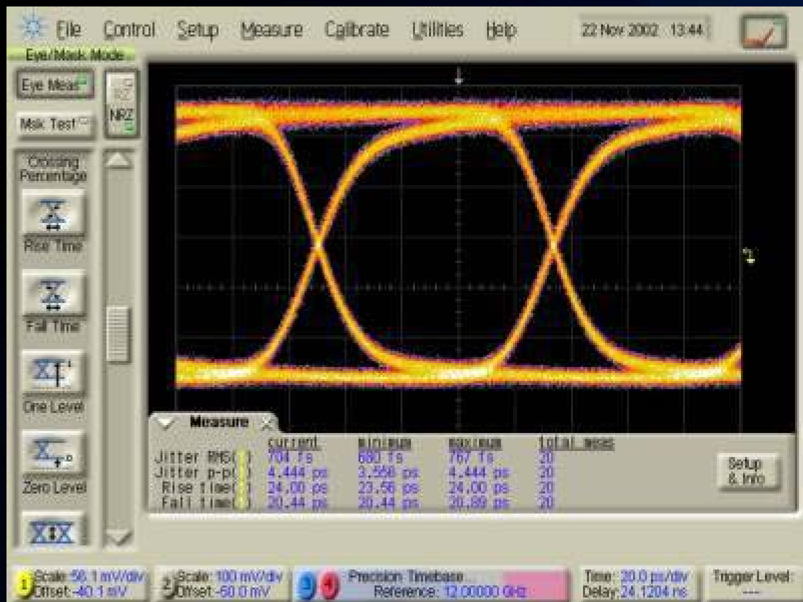
Inphi®
Think fast.

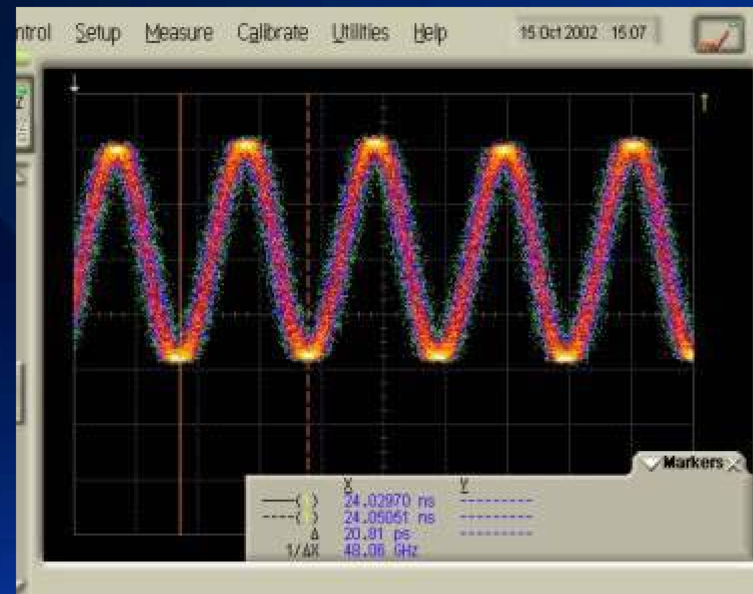
InP Technology for High-Speed ICs (con’t.)

- Gold interconnect
- Semi-insulating substrate
- Low-k dielectric
- Backside vias available
- Currently 1 μm feature size
  - Easily scaled to smaller geometries
  - Inexpensive
  - Limited number of process steps
- Limited integration

Inphi® Think fast.

High-Speed Circuit Examples



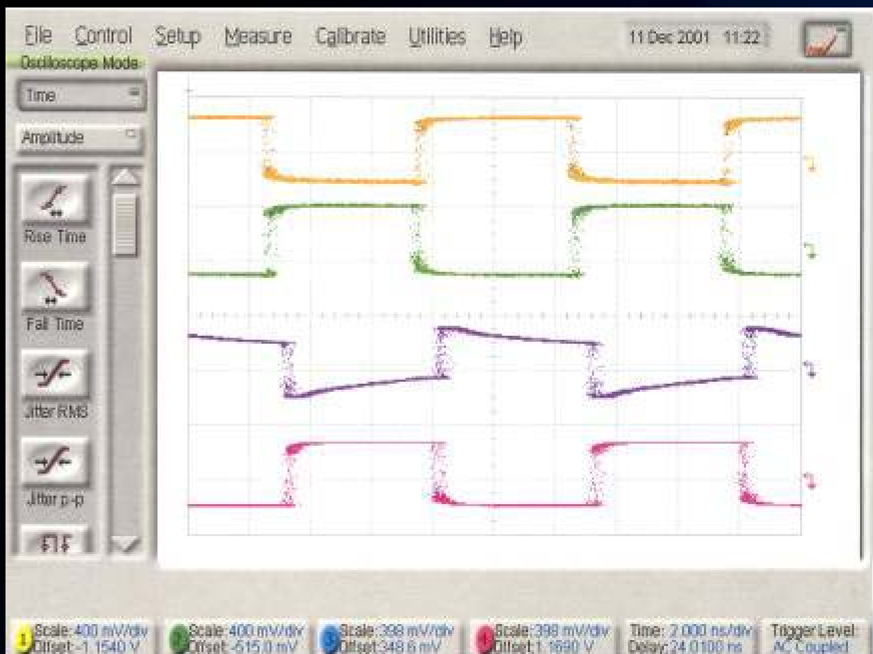


10 Gbps CMOS
1:4 Demux + 4:1 Mux
Back-to-Back
~300 mW

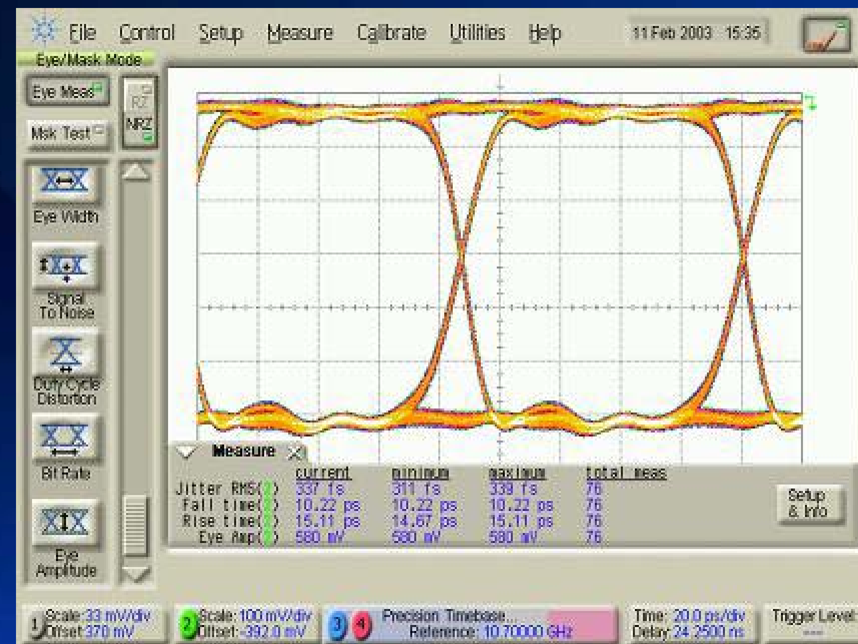
96 GHz InP
Static Divide-by-2
~150 mW

Inphi®
Think fast.

InP High-Speed Circuit Examples



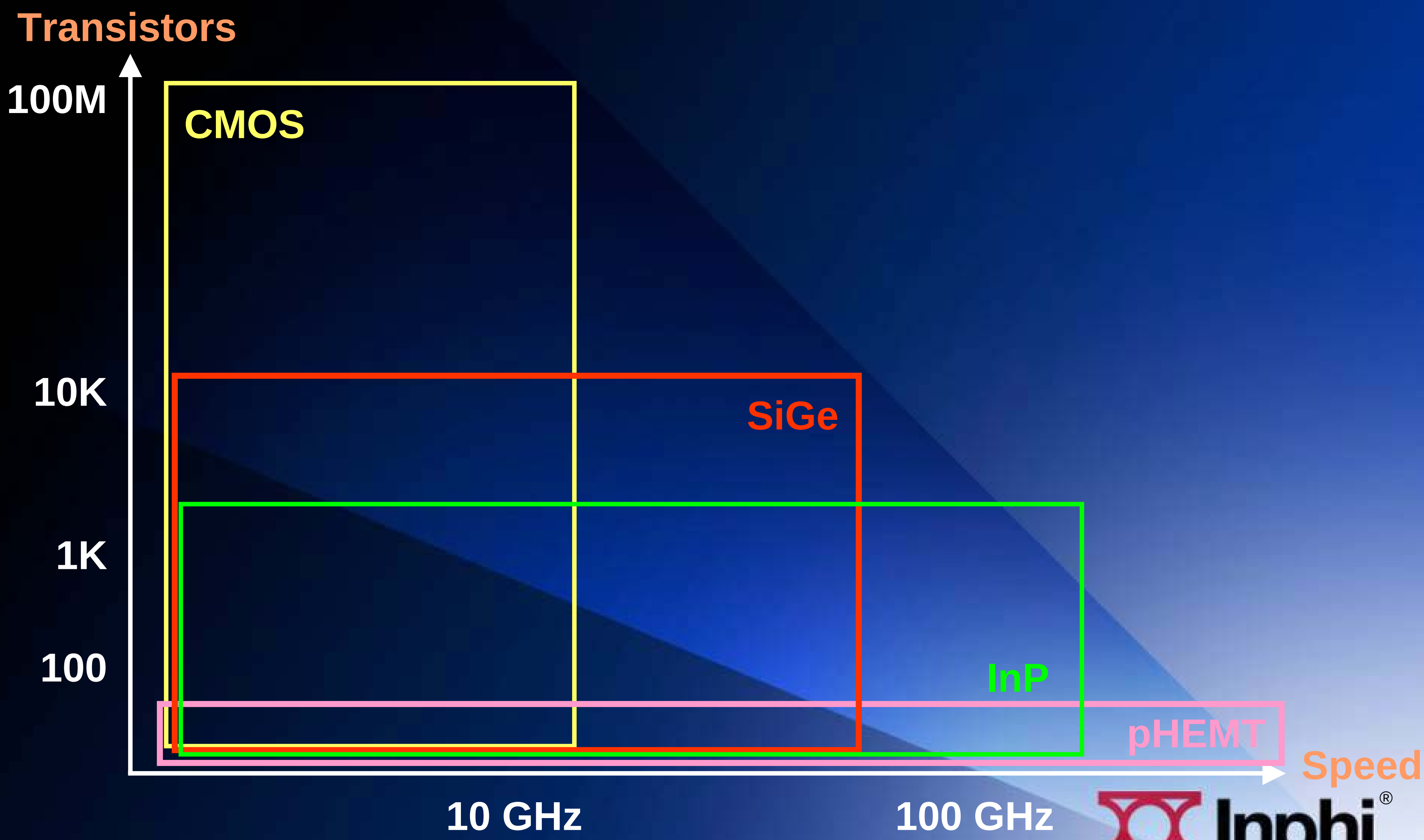
1:4 Demux
Operation at 80.6 Gbps
Beat Test



13 GHz D flip-flop
~0.3 ps jitter rms
~10 ps rise/fall time

Inphi®
Think fast.

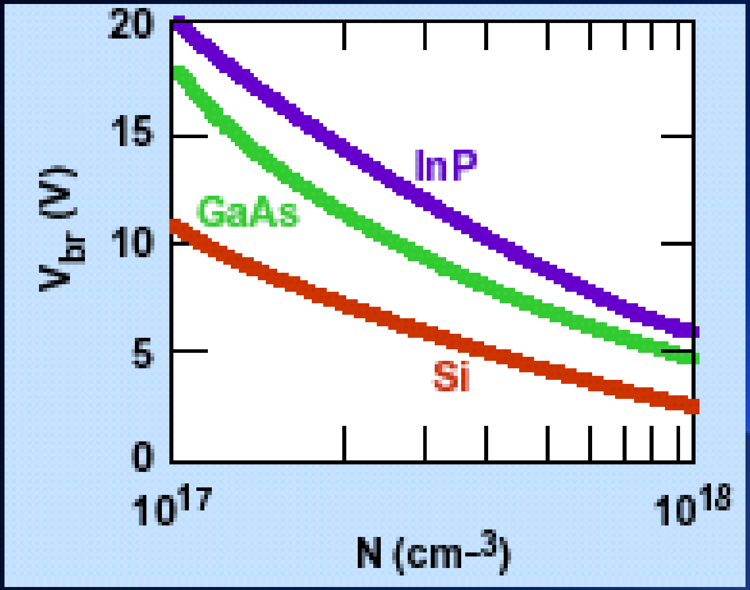
Complexity / Speed Tradeoff

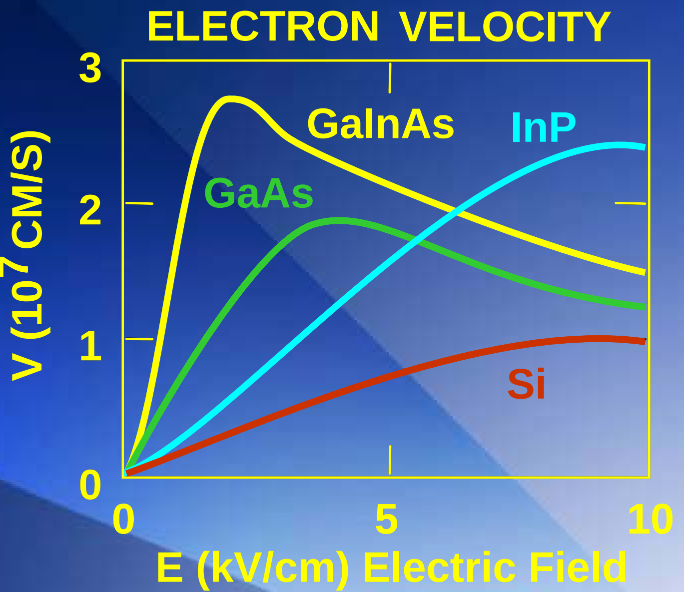


Inphi® Think fast.

Voltage Swing / Speed Tradeoff

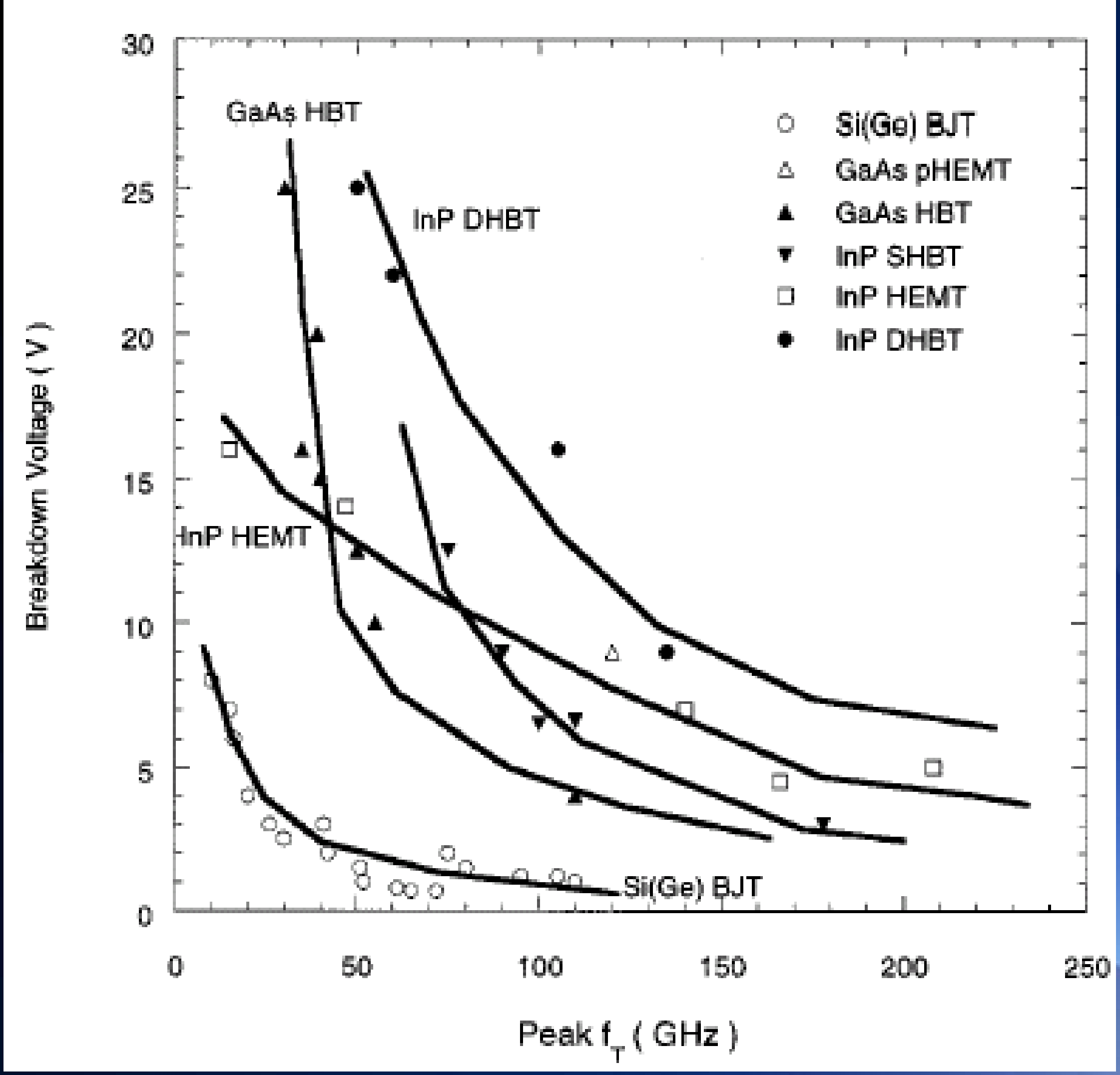
- InP has higher electron velocity and breakdown voltage than silicon
- For same speed, t_{coll} (Si) < t_{coll} (InP)
- InP devices have higher breakdown for same speed
- Alternatively, InP devices are faster for same breakdown



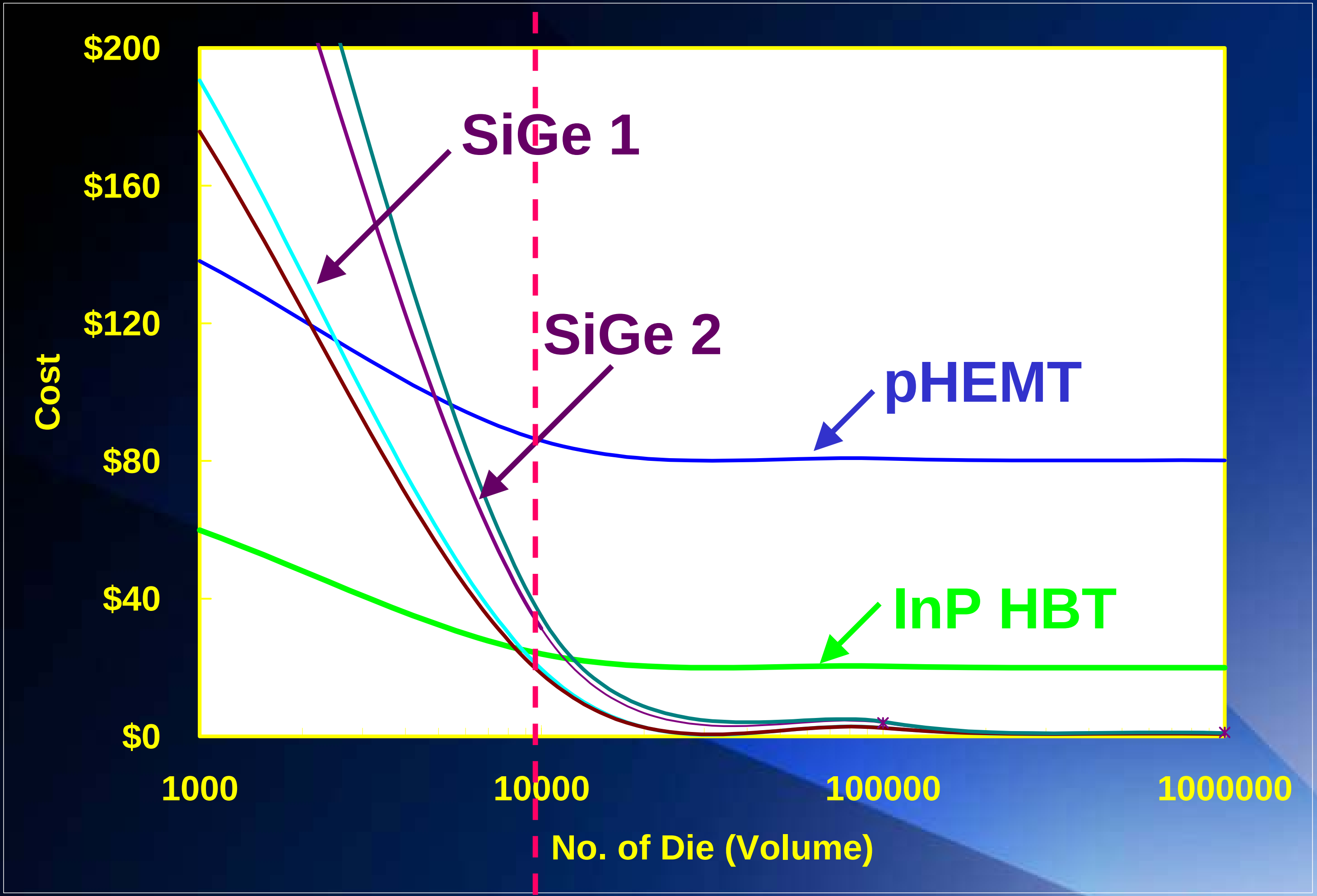


Inphi®
Think fast.

Breakdown Voltage / Speed Tradeoff



Cost Tradeoffs



Mask cost limited | Yield / wafer size limited

Inphi® Think fast.

Device Requirements for Optical Mach-Zehnder Drivers

- High voltage swing (~7 V p-p, 12.5 Gbps)
- High breakdown voltage (> 8 V)
- High speed (f_t > 100 Ghz)
- Technology choices
  - GaAs pHEMT
  - GaAs bipolar
  - InP DHBT (Inphi choice)

Inphi® Think fast.

Technology Comparison

	GaAs pHEMT	GaAs HBT	InP DHBT
Device Speed / Performance	2	1	4
Power Dissipation	5	1	4
Die Size	2	4	5
Reliability	4	3	4
External Components	1	4	4
Gain	1	5	5

1-5 scale, 5 = best

Inphi®
Think fast.

Reliability

- Process reliability varies from CMOS (extremely mature) to InP DHBT (relatively new)
- Foundry evaluation should include detailed reliability evaluation
- Mature foundry should have reliability data on actives and passives and design rules for reliability
- Much of this information is proprietary

Conclusions

- Numerous choices for high-speed process technologies
- Choose the optimal process for a particular application
- In general, the newer the process, the more time required to get it into production

Presenter Biographies

Dr. Gopal Raghavan, CTO. Dr. Gopal Raghavan has over 20 years of experience in high-speed circuit design and device modeling. From 1982 to 1994, Dr. Raghavan was a senior engineer with Intel Corporation engaged in CMOS circuit design and process development. Prior to founding Inphi, Dr. Raghavan was a principal engineer at Conexant designing integrated circuits for 10 Gbps SONET applications. Dr. Raghavan has won several awards, including the Hughes Hyland Patent Award (1998) and the Ross Tucker Award from TMS/IEEE (1993). He holds 10 patents and has published more than 30 technical publications. Dr. Raghavan holds M.S. and Ph.D. degrees in electrical engineering from Stanford University as well as a B. Tech degree in electrical engineering from the Indian Institute of Technology.

Inphi®
Think fast.