

## Measuring Maximum Variation in Clock Delay on the DDR3 Registering Clock Driver

The maximum variation in clock delay between the input and output for DDR3 Registered DIMMs is a critical device parameter that if not observed, could cause system failures. After write-leveling is performed in the system, the clock to the DRAMs must be relatively stable over voltage and temperature variation in order to maintain timing margins.

The maximum variation in the clock delay between the input and output ( $t_{DYN\text{OFF}}$ ) is a measure of the PLL's stability and should not exceed the DDR3 SSTE32882 JEDEC specification.

Table 1. Clock Driver Jitter Characteristics

Symbol	Parameter	Conditions	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{FDYN}$	Dynamic phase offset		-50	50	-50	50	-50	50	-40	40	ps
$t_{STAOFF}$	Average delay through the register between the input clock and output clock <sup>5</sup> (1.5 V Operation)	Standard ½-Clock pre-Launch $T_{STAOFF} = T_{PDM} + 1/2 T_{CK}$	1.90	2.25	1.59	1.94	1.40	1.75	1.28	1.63	ns
	Average delay through the register between the input clock and output clock <sup>5</sup> (1.35 V Operation)	Standard ½-Clock pre-Launch $T_{STAOFF} = T_{PDM} + 1/2 T_{CK}$	1.90	2.45	1.59	2.14	1.40	1.95	1.28	1.83	ns
$t_{DYN\text{OFF}}$	Maximum variation in delay between the input & output clock		-	160	-	130	-	110	-	90	ps

It is important to accurately measure  $t_{DYN\text{OFF}}$  to ensure the system will not encounter failures due to the integrated PLL of the SSTE32882. Figure 1 shows the timing relationship between the input and output clocks with respect to the  $t_{DYN\text{OFF}}$  parameter.

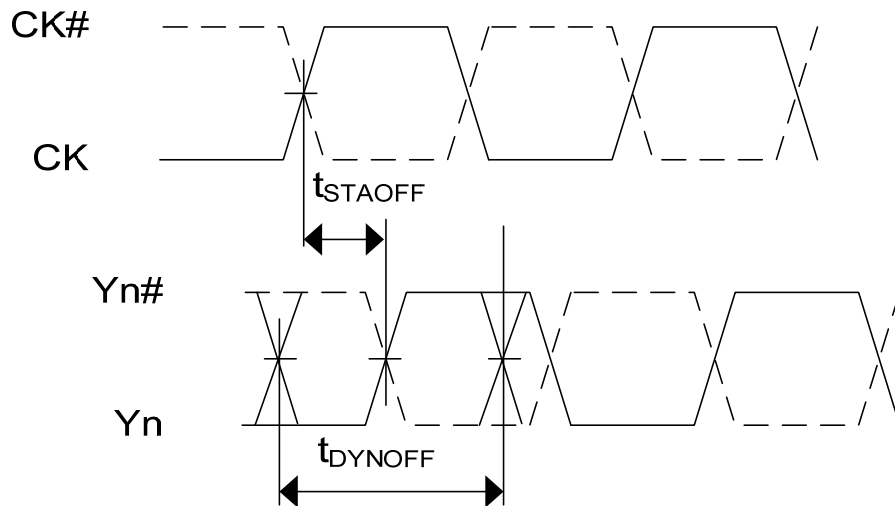


Figure 1.  $t_{DYNOFF}$  timing diagram of input clock and output clock

### Definitions:

$t_{STAOFF}$  - propagation delay between the Register PLL's input and output clock measured over N cycles

$t_{DRIFT}$  - deviation in static phase offset with respect to the average  $t_{STAOFF}$  over voltage and temperature

$t_{DYNOFF}$  - maximum variation of  $t_{STAOFF}$  (includes noise sources ie jitter, SSC, SSO, etc)

The proper procedures to accurately measure the maximum variation in clock delay between the input and output clocks are as follows.

### Recommended Equipment:

An oscilloscope with a bandwidth of at least 6 GHz, 12 GHz being ideal, should be used to minimize signal attenuation. Along with the oscilloscope, differential probes with at least 6 GHz bandwidth, 12 GHz being ideal.

DDR3 system with voltage margining tools or register/clock reference board. If using a register/clock reference board, ensure that the source clock exhibits period jitter of no more than 5ps rms in order to minimize jitter transfer.

A temperature chamber or some sort of temperature forcer to vary the temperature. A thermocouple to measure the temperature of the DUT

### Measurement Procedure:

Probe and trigger on the differential source clock (aka reference clock) to the DDR3 Registering Clock Driver at or very near the termination resistor on the registered DIMM.



Think fast.

Probe the differential output clock (aka DRAM clock) of the DDR3 Registering Clock Driver at or very near the termination resistor on the registered DIMM.

Start off by setting the power supply voltage ( $V_{DD}$ ) to the RDIMM and temperature ( $T_{CASE}$ ) to a VT corner. Set the oscilloscope for infinite persistence. Clock drift over VT corners, tracking error, and jitter are all captured at once using infinite persistence. Zoom in on the rising edge of the output clock and set X-cursors on the left and right side of the output waveform at the 0V crossing. Figure 2 shows the input clock as the blue trace and output clock as the red trace.

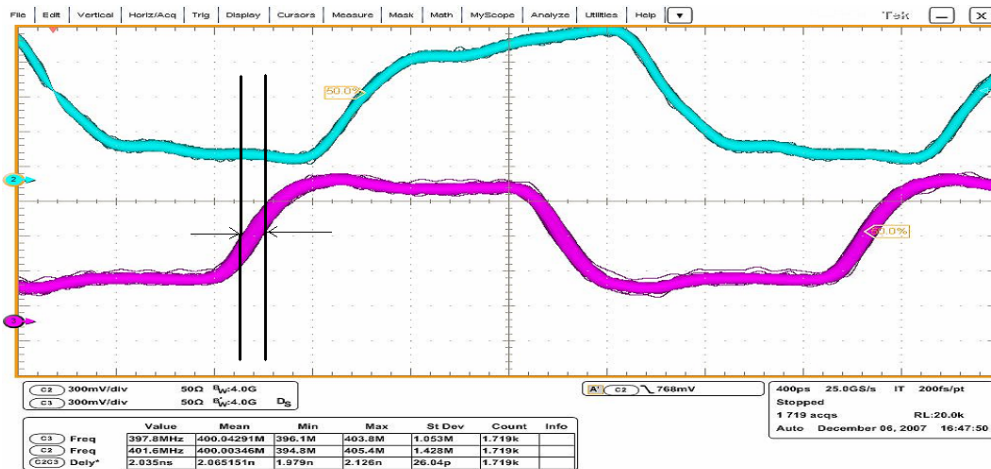


Figure 2. Infinite persistence waveforms of input and output clock

There are basically two VT corner cases, fast and slow, that will determine the  $t_{DYN\text{OFF}}$  of the SSTE32882 device. For the fast VT corner case, set the power supply voltage to the RDIMM to the maximum limit of the operating range. Next, set the case temperature to the minimum operating condition. A thermocouple should be used to measure  $T_{CASE}$ . Record the measurement data after about a minute at the fast VT corner. Next, measure the slow VT corner case by lowering the voltage to the minimum limit of the operating range and raising  $T_{CASE}$  to the maximum operating condition. Record the measurement data after about a minute at the slow VT corner.

Figure 3 is a statistical illustration of  $t_{DYN\text{OFF}}$ .

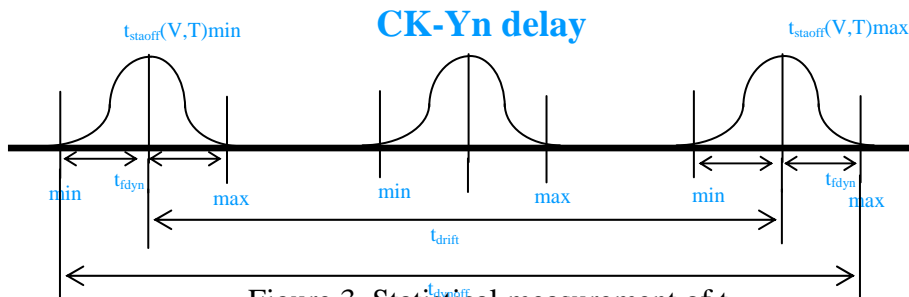


Figure 3. Statistical measurement of  $t_{DYN\text{OFF}}$



*Think fast.*

$$t_{\text{DRIFT}}(V, T) = t_{\text{STAOFF}}(\text{max}) - t_{\text{STAOFF}}(\text{min})$$

$$t_{\text{FDYN}} = t_{\text{JIT}} + t_{\text{TRACK}}$$

$t_{\text{TRACK}}$  is the PLL's tracking error of the input clock with SSC either on or off

$t_{\text{JIT}}$  is the intrinsic jitter from the PLL

The  $t_{\text{DYNOFF}}$  measurement procedure described provides repeatable and reliable results to ensure a stable PLL and system.