

Operating the Inphi DDR2 and DDR3 PLL in Bypass Mode

Memory module manufacturers find it more and more difficult to be able to production test hundreds of registered DIMMs using ATE. One factor that makes it difficult is the PLL clock buffer, which has a relatively higher application/operating frequency range in DDR2 and DDR3 than most ATEs are capable of.

The PLL clock buffer is used to buffer and distribute the memory controller clock to all the DRAMs and/or register on the RDIMM with an operating frequency ranging from 200 MHz up to at least 800 MHz. However, the clock buffer will also need to operate at very low frequencies ie <90Mhz for testing purposes. It becomes difficult to design a stable PLL with a wide enough operating frequency range and still meet PLL timing per JEDEC specifications.

To address this, Inphi has designed the PLL to operate at frequencies below the application frequency range without interruption to the ATE. In both DDR2 and DDR3 RDIMM applications, the PLL is able to go into PLL bypass mode (or buffer mode).

DDR2:

The Inphi INCUA877-GS04 and INCUA845 are JEDEC standard DDR2 PLL clock buffers (JESD82-18A) that has an added feature of automatically switching over to buffer mode for low frequency testing. Once the input clock frequency falls below a threshold of 90 MHz, the PLL is bypassed and running in buffer mode, which is able to operate at frequencies in the Hz. Per the JESD82-18A specifications, the input clock slew rate (single-ended) must be ≥ 1 V/ns and input common mode $\geq V_{DD}/2 - 0.15$ V for proper operation.

DDR3:

The Inphi INSSTE32882 is a JEDEC standard DDR3 Registering Clock Driver where the PLL is still present but integrated with the register as a single chip design. The frequency band 2 of the INSSTE32882 allows low PLL lock frequency down to 70 MHz. The INSSTE32882 is a programmable register enabling or disabling specific modes of operation and/or device features via internal control bits. There are 16 words of control bits (RC0... RC15) accessible in a specific mode of operation that is described in the specification document. RC0 through RC5 and RC8 through RC11 are JEDEC defined but RC6, RC7, and RC12 through RC15 are reserved words. Inphi has added extra devices features that can only be enabled via the reserved words. One extra device feature is for forcing the chip into PLL bypass mode for low frequency operation. RC7 and RC14 are the two words that need to be programmed to enable this mode. The Control Word Decoding table shows the address and configuration of RC7 and RC14 to force the INSSTE32882 into buffer mode.

Control Word Decoding Table

	Control Word Address				Control Word Value				
Control Word	DBA2	DA2	DA1	DA0	DBA1	DBA0	DA4	DA3	Meaning
RC7	L	H	H	H	1	0	0	0	PLL bypass mode
RC14	H	H	H	L	0	1	0	0	PLL bypass mode

In order to successfully configure the control bits, the programming needs to be done after RESET# is de-asserted and stabilization time is met. The control bits will default to “0” every time the chip is reset. In PLL bypass mode, the INSSTE32882 can operate below 70MHz.

The alternative to forcing the DDR2 and DDR3 PLL into bypass mode is by setting AVDD (analog power supply to the PLL) to ground.