Deployment of 100G in the Metro Network, Applications and Drivers

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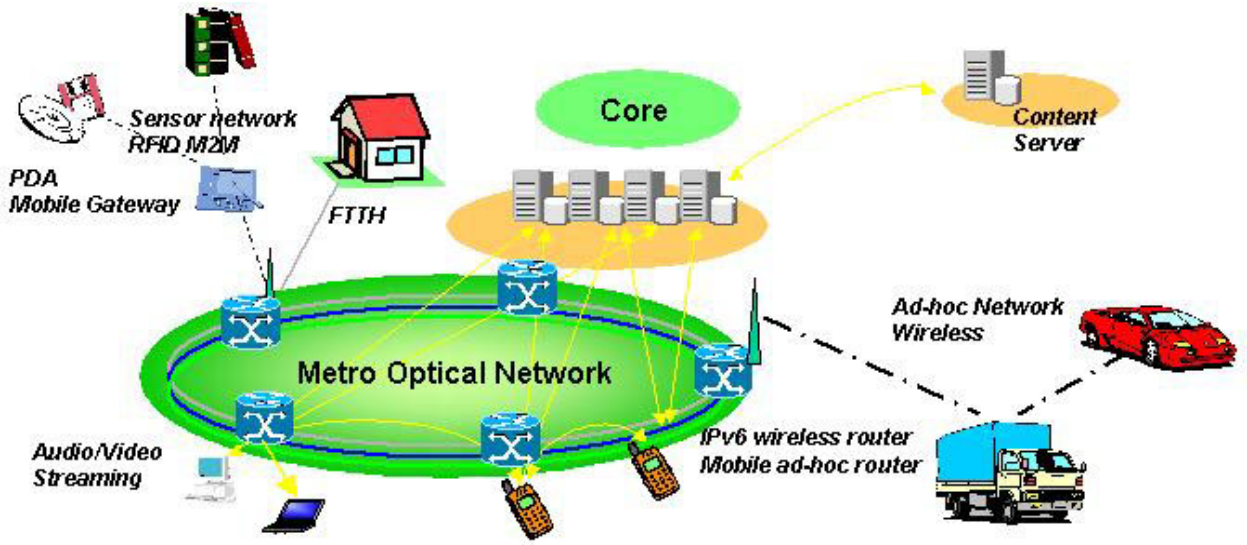
Overview

Explosive growth in mobile data traffic, data centers, and cloud services are the catalyst behind the significant traction of 100G and it's deployement by major carriers worldwide. Two enabling drivers are the commercialization and availability of 100G OTN/Ethernet merchant silicon and 100G DP-QPSK Coherent modules.

100G rates were initially deployed in the Long Haul and Core networks. In the Metro, 10G is still the most dominant rate. In the coming years, the trend toward aggreagation into 100G in the larger metro areas or data center connectivity will become more significant. Metro networks characteristics dictate lower distances (vs. Long Haul/Core), more flexible protocol support, higher granularity of signal rates, and increased number of nodes. These characteristics create a set of different requirements for optical modules, and merchant silicon for mapping, aggregation and transport of 100G rates.



Picture 1: Typical Metro Network

Metro Networks Characteristics

Metro Networks characteristics may be categorized into three general areas:

1. Connectivity
2. Architecture
3. Protocol

The following sections examines each area in more detail, and looks at how Cortina's line of OTN processors and FEC families supports these requirements.

1. Connectivity

Metro networks typcially have much shorter distances but much higher number of nodes. 100G Coherent optical modules, used in the core and submarine applications, are simply too expensive, too big, and consume too much power for these type of networks. These modules typically incorporate a Soft Decision (SD) based Forward Error Correction FEC implemented in a Digital Signal Processor (DSP). This approach provides more granular adjustable Net Coding Gain at different overhead rates compared to traditional Hard Decision (HD) based FEC but at a cost of more power and latency.

Next generation optical modules based on CFP2 and CFP4 form factors are designed to fill this gap with much lower power and smaller profile. For instance, the maximum power specified for CFP, CFP2, and CFP4 are 32W, 12W, and 5W respectively. The CFP form factor is flexible and currently supports both 40G and 100G rates with 10x10G or 4x25G host interface but it's relative size and complexity limits it's future in the Metro networks. The CFP2 and CFP4 form factors with native support for 4x25G interface are better suited and will become the dominant form factors. Current solutions in the market require "gearbox" chips which significantly increase power, space, and cost. Cortina's fourth generation OTN Processor family will incorporate native support for 25G I/O eliminating the external "gearbox" chips thereby providing the most optimized solution supporting these form factors.

First generation CFP2 and CFP4 modules will most likely incorporate direct detect modulation. A Soft Decision DSP based FEC consumes too much power and not suitable for these form factors today. More efficient next generation coherent technology may eventually find it's way into these modules as the technology matures in the next few years. Using a high performance Hard Decision (HD) based FEC with direct detect modulation provides a more optimal

cost/perforamce ratio meeting the lower power and latency requirements for metro applications. The current standard G.709 (RS-255, 239) HD based FEC provides 6.7% Net Coding Gain (NCG) at 7% but this performance is not adequate for today's network. Although higher performance FEC algorithms have been introduced over the past few years by several vendors supporting 40G and 100G rates, all are proprietary implementations.

A higher performance standard based FEC is therefore highly desirable, not only meeting the performance requirements of today's networks at higher signal rates, but also meet multi-vendor interoperability requirements desired by major service providers.

High Gain FEC (HG-FEC)

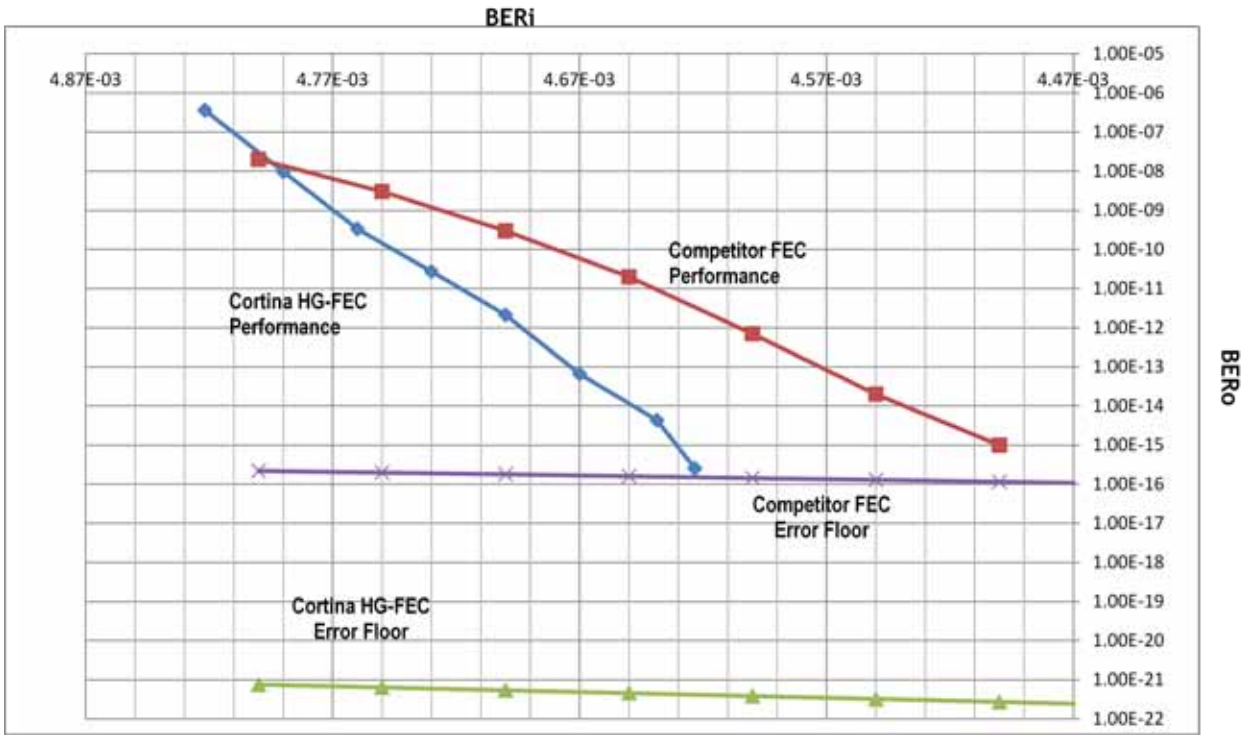
In 2011, Cortina introduced a best in class, high performance FEC (HG-FEC) with the introduction of the CS605x 100G ASSP OTN processor and FEC family. This HD based FEC provides best in class 9.4dB NCG at 6.7% Overhead with lowest error floor rate in the industry today. The "Staircase" scheme provides the required reach and performance at a substantially lower cost and power when compared to SD based FECs used for 100G Long Haul applications. Furthermore, this FEC can provide the same performance for beyond 100G future.

Below are the feature highlights of this FEC:

- 9.4dB NCG for output error rate of 1E-15 with 6.7% overhead
- Low Latency of 16.2us in the High-Gain mode. Flexible decoder can trade off between latency and coding gain
- Optional Error Decorrelator for compatibility with 100G DP-DQPSK or other 100G modulations
- Uses highly iterative codes to increase the coding gain with systematic mapping same as GFEC Standard
- Accurate error reporting including corrected 1s and 0s count in addition to uncorrectable block count. Standard error statistics like signal-fail and signal-degrade and input bit-error rate is supported
- Proven functionality in silicon and deployed in multiple networks since 2012

Error Decorrelator

- An optional Error-Decorrelator has been added to the FEC system to maintain good error correction capability when the input errors are correlated
- The large interleaving depth of the error decorrelator(>2K bits) results in robust error correction capability in many Fiber communication systems that produce correlated errors
- Even with the Error-Decorrelator turned on, the FEC code is still systematic and OTU4 frame compatible



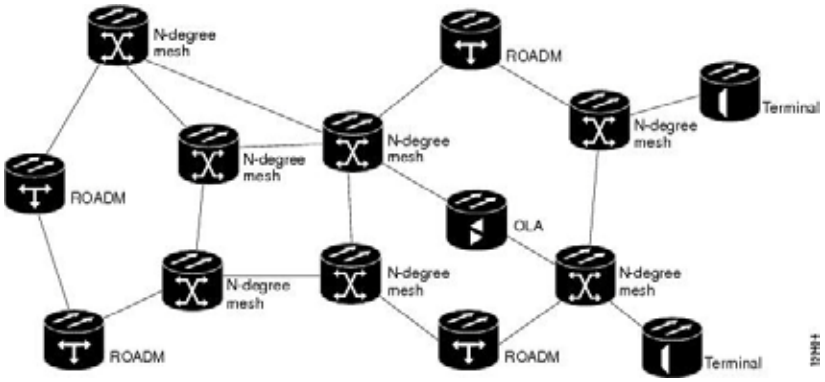
Picture 2: HG-FEC Comparison Chart

ITU-T Standardization

Cortina has submitted this FEC as a proposal for standardization into ITU-T for OTU4 and beyond 100G Multi Vendor activity. Furthermore, Cortina intends to propose a license and royalty free fee model for use by component vendors, system manufacturers, and service providers. Additional information regarding detail performance and feature is available from ITU-T website.

2. Architecture

Typical metro networks incorporate a mesh architecture (Picture 3) with protection paths. Aggregation and multiplexing of lower signal rates into higher rates is a requisite with the ability to add/drop clients at both wavelength and service levels at each node. Requirements include support for finer granularity signal rates such as ODU0, and multi-stage multiplexing.



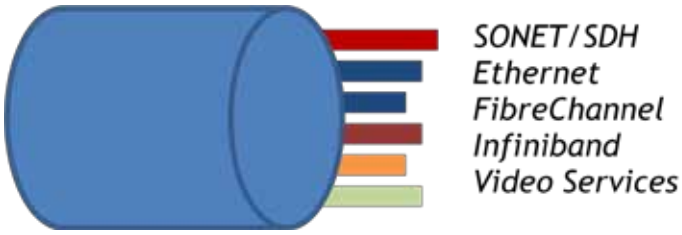
Picture 3: Example of Metro Mesh Architecture

With the introduction of ODU0 and ODUflex into the OTN hierarchy, existing networks need to incorporate facilities to support these smaller granularities efficiently. Multi-stage multiplexing is a scheme that allows more efficient transport of these signals. For example, ODU0 is mapped first into ODU1 or ODU2 and ODU1/2 is then mapped into ODU3.

Cortina's fourth generation Optical Transport Processor and FEC Device family incorporates five stage multiplexing, support for OTN switching, and OTN SAR for packet over OTN transport applications.

3. Multiple Protocols

Metro networks have connections to a variety of network types including Core (Long Haul), Access, Mobile Wireless, and Enterprise. These networks drive Data Centers, and Cloud based applications and services, which require the network equipment and line cards to be capable of supporting different clients, protocols and line rates (Picture 4).

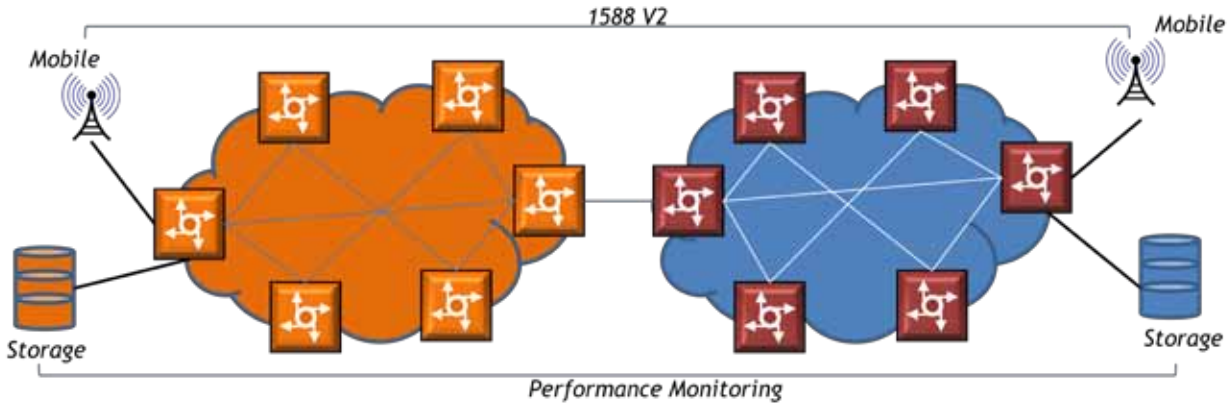


Picture 4: Multiprotocol Support

Efficient mapping and transport of these clients through the OTN network is critical. Two basic type of clients needs to be supported: Constant Bit Rate (CBR) or TDM based clients. Mapping and transport of CBR clients such as FibreChannel, Infiniband, and CPRI is supported through the OTN network using several mapping options such as BMP, AMP, GMP, or GFP as per ITU G.709 and G.SUP43 standards. Mapping and transport of TDM clients, such as SONET/SDH, or packet clients, such as Ethernet (10GE, 40GEe, 100GE), MPLS-TP, RPR, and IP/PPP, is also supported through Generic Framing Procedure (GFP-F) mapping.

Cortina's CS600x OTN processor and FEC device family introduced in 2008 was the first merchant silicon capable of mapping and transporting independent client protocols simultaneously at 10G and 40G rates for OTN, SONET/SDH, Ethernet, FibreChannel and Infiniband. Cortina's current and next generation OTN processors families incorporate high performance Serializer/Deserializer (SERDES) for direct connection and native support of various clients, optical modules, supporting all latest bit rates and meeting the stringent requirements of each protocol such as jitter, and timing.

In addition to mapping and transporting of these protocols, end clients, such as data centers and service providers, require facilities for performance monitoring. Also Mobile Cellular networks are increasingly using the IP network for backhaul and connectivity of voice services due to lower cost and easier management. Supporting the precise time synchronization between the radio networks is another key requirement (Picture 5).



Picture 5: Example of End-to-End Performance Monitoring

Cortina's OTN processors support transparent and non-intrusive performance monitoring in both Ingress and Egress directions for all clients mentioned above and also provide support for IEEE 1588V2 Precision Time Protocol for mobile backhaul applications.

Summary

Explosive growth in mobile data traffic, data centers, and cloud services are the catalysts behind significant traction of 100G deployments in the Core and Long Haul networks. Service providers and carriers are accelerating the deployment of 100G but also looking carefully to manage their CAPEX and OPEX effectively.

Next generation optics and merchant ASSP silicon provide the key drivers for providing higher efficiency, more capacity, and lower cost solutions. Cortina Systems is working closely with Carriers, Network Equipment Manufacturers, Optical Module Suppliers, and Standardization bodies to provide highly integrated, high performance merchant silicon for next generation Optical Transport Networks.