13.6 A Fully Integrated 43.2Gb/s Clock and Data Recovery and 1:4 DEMUX IC in InP HBT Technology

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Future growth of optical communications infrastructure will drive state-of-the-art components to 40Gb/s. Greater signal degradation at 40Gb/s, in electrical circuits and optical media, favors forward error correction (FEC) and an even higher bit rate (43Gb/s) to support the FEC overhead. A 43.2Gb/s clock and data recovery (CDR) and 1:4 DEMUX IC is described. This may be combined with a 4:16 CMOS deserializer to realize the industry-standard SFI-5 1:16 deserializer which combines the respective strengths of InP and CMOS technologies. The result is high-speed performance and efficient implementation of moderately high-speed parallel circuitry.

The CDR/DEMUX IC is implemented in a production InP HBT process [1], with 100mm wafer size and 1μm emitter width. The process includes HBT's, varactors, thin film resistors, and MIM capacitors, with two-layer gold interconnect in low-k dielectric. Fabricated HBT's have 150GHz f_t and 170GHz f_{max} at 1mA/μm^2 current density and 1V collector-emitter voltage.

The IC is a fully integrated CDR/DEMUX unit, requiring only a single external capacitor for complete functionality and operates from an industry standard +3.3V supply. Figure 13.6.1 depicts a block diagram of the IC.

An integrated broadband limiting amplifier enhances input sensitivity. The limiting amplifier drives a half-rate clock interleaved version of an Alexander phase detector (PD)[2,3]. Interleaving in the PD realizes a 1:2 DEMUX. The data outputs of the PD drive a 2:4 DEMUX to complete the data path.

The clock recovery phase-lock loop (PLL) consists of the PD, a proportional and integrating (PI) loop filter, a VCO, and a frequency divider. Clock recovery uses a "bang-bang" type PLL, because the phase detector produces binary-quantized phase error outputs [4]. A parallel clock multiplier loop can lock the VCO to a multiple of an external reference clock. The parallel loop shares the PI filter, VCO, and frequency divider with the clock recovery PLL, and adds additional frequency dividers, a frequency lock detector and an acquisition aid. The frequency lock detector determines whether a divided version of the recovered clock is within a +/-1000 ppm frequency window about the reference clock. If the recovered clock falls outside the window, the lock detector activates the clock multiplier loop. The clock multiplier loop has higher loop bandwidth to override the clock recovery circuitry and speed up frequency acquisition. The frequency lock detector has hysteresis for a clean transition of loop control from clock multiplier to clock recovery circuitry.

The Alexander PD has several benefits for high operating speed and low jitter, including: combined input retiming / phase detector functionality which inherently optimizes retiming clock alignment; output pulses with a fixed width, which reduces the required circuit bandwidth; and tristate output, which prevents excess jitter with consecutive identical digits in the input bit stream. Interleaving allows a lower rate clock, which reduces data retiming metastability and enhances the sharpness of the binary-quantized phase detector error outputs.

The VCO uses a ring oscillator topology which conveniently permits separate coarse and fine tuning for the respective integral and proportional feedback paths of a bang-bang PLL [4]. Current starving is used for the small-scale, fast-changing proportional tuning, while delay interpolation is used for the larger-scale, slower-changing integral tuning.

Circuit broadbanding techniques are essential to achieve good performance without excessive power dissipation in the limiting amplifier and the 43GHz frequency divider. Bandwidth is broadened by shunt and series peaking, use of transadmittance-transimpedance stage cascades [2] and careful design of interconnect. Interconnect design includes selecting a geometry for a specific wave impedance and optimizing terminating impedances for signal voltage transfer. Figure 13.6.2 illustrates one stage in the limiting amplifier that uses shunt peaking and the transadmittance-transimpedance cascade. Shunt peaking and interconnect design minimize the propagation delay of latches comprising the frequency divider and ensures its performance over the entire range of operating conditions.

Latch propagation delay governs performance of the phase detector. A split load resistor technique, illustrated in Fig. 13.6.3, reduces latch propagation delay. The ECL latch has one differential pair for tracking the input, and another for latching the output. Separate emitter follower pairs are used for feedback and propagation taps at different points of the split load resistor. This separates the capacitance of the tracking and latching differential pair outputs, as well as for the propagating and regenerating emitter follower inputs. By virtue of isolation from the load capacitance of the latching pair, the tracking pair propagates a stronger signal with less delay. The Miller capacitance of the regenerating pair is reduced, allowing the latch to more quickly resolve internal metastability.

Circuit performance is measured on wafer with the external chip capacitor mounted on the wafer probe card. The measurements are made at +3.3V and do not significantly change +/- 5% supply variation. The power dissipation is 3.3 W and the die area is 10.2mm^2.

Figure 13.6.4 shows the recovered clock spectrum and demultiplexed data waveforms. The rms jitter of the recovered clock, corrected for oscilloscope trigger jitter, is less than 1 ps. The measured input sensitivity for BER below 10^{-12} is 27mVp-p differential. The jitter tolerance is measured in two steps because of the limited modulation bandwidth of the pattern generator clock source. For lower frequency jitter, the pattern generator clock source is directly phase modulated by sinusoidal signal. For higher frequency jitter, a balun is used to add a slightly frequency-detuned, low amplitude sinusoid to the unmodulated clock sinusoid. The sum of the two signals is a clock with low jitter amplitude and jitter frequency equal to the frequency detuning of the low amplitude source. Figure 13.6.6, shows the measured jitter tolerance exceeds an extrapolated SONET OC-768 jitter tolerance mask (OC-192 jitter tolerance mask frequencies quadrupled), and achieve better than 0.43 UI_{pp} high frequency jitter tolerance.

References

[1] Nguyen, N.X. et al., "Manufacturable Commercial 4-inch InP HBT Device Technology," *2002 GaAs MANTECH Conf. Digest,* pp.26-29, Apr. 2002.

[2] Reinhold, M. et al., "A Fully-Integrated 40Gb/s Clock and Data Recovery / 1:4 DEMUX IC in SiGe Technology," *ISSCC Digest of Technical Papers,* pp.84-85, Feb. 2001.

[3] Alexander, J.D.H., "Clock Recovery from Random Binary Signals," *Electronics Lett.*, pp.541-542, Oct. 1975

[4] Lai, B., Walker, R.C., "A Monolithic 622mb/s Clock Extraction Data Retiming Circuit," *ISSCC Digest of Technical Papers,* pp.144-145, Feb. 1991.

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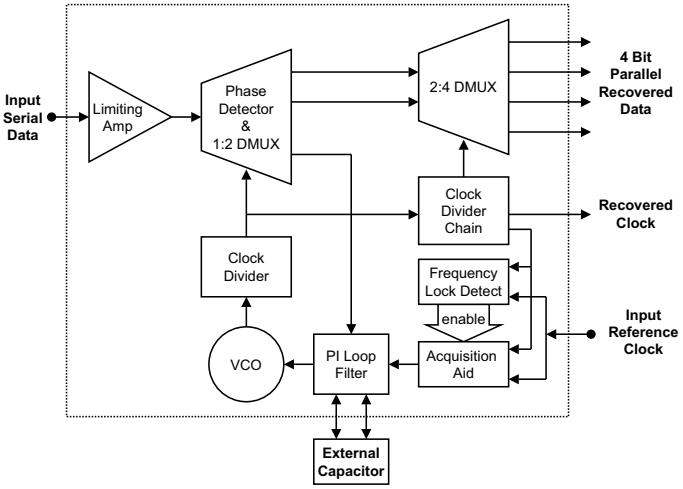

Figure 13.6.1: IC block diagram.

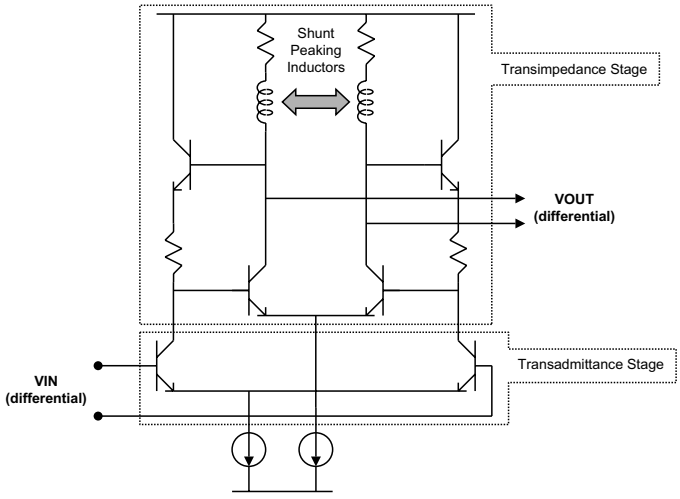

Figure 13.6.2: Limiting amp broadband gain stage schematic.

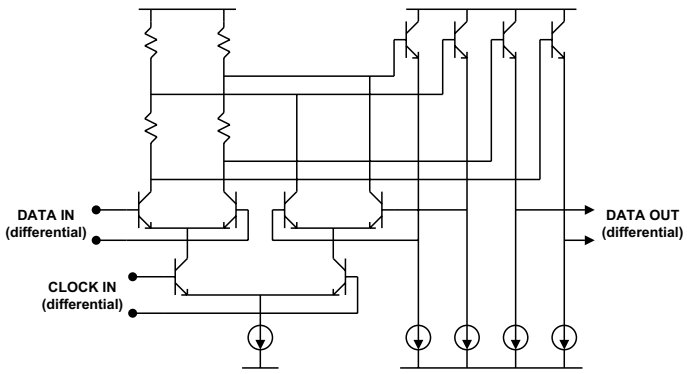

Figure 13.6.3: Split load resistor latch schematic.

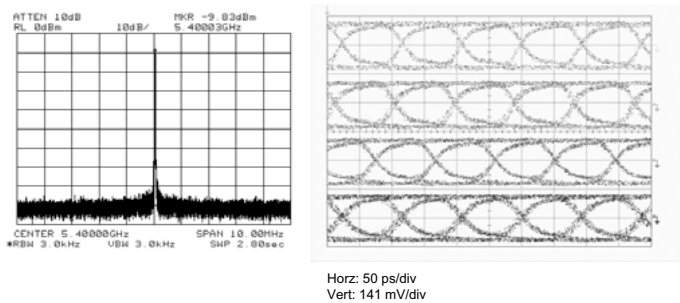

Figure 13.6.4: Recovered clock and demultiplexed data outputs.

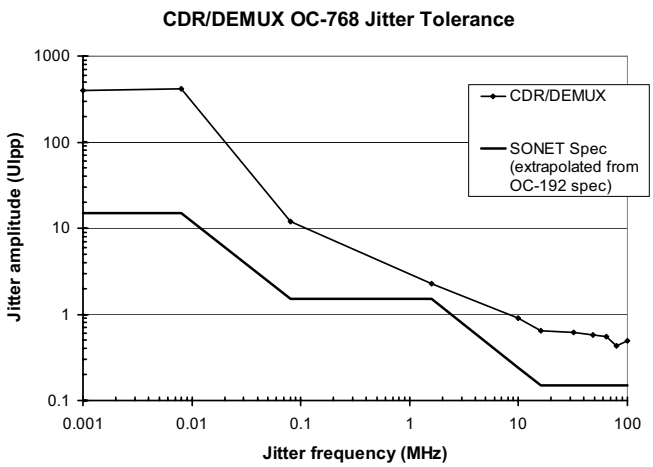

Figure 13.6.5: Measured jitter tolerance.

Technology	InP HBT, 2 metal, low-k dielectric
Supply Voltage	+3.3 V, +/- 5%
Power Dissipation	3.3 W nominal
Chip Size	3.2 mm x 3.2 mm
Input bit rate	39.8 - 43.2 Gbps
Output bit rate	9.95-10.8 Gbps
Recovered clock frequency	4.975-5.4 GHz
Measured input sensitivity	27 mVpp differential
Measured recovered clock jitter	850 fs rms
Measured jitter tolerance	Exceeds extrapolated Telcordia GR-253 CORE mask
Measured jitter transfer peaking	< 0.1 dB

Figure 13.6.6: IC characteristics summary table.

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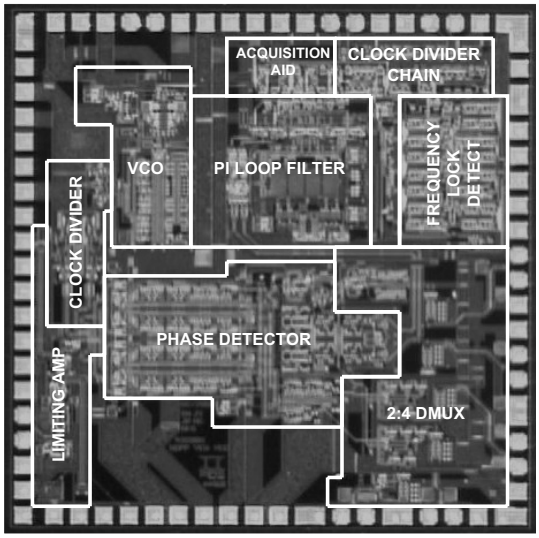

Figure 13.6.7: Die microphotograph.