Frequency Domain Measurements for High-Speed PMD Integrated Circuits

Dr. Carl Pobanz, Principal Design Engineer

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Frequency Domain Measurements

- **Discussion will focus on network analysis for 10 & 40 Gb/s lightwave physical media–dependent (PMD) ICs**
  - **Data amplifiers, modulator drivers, TIAs**
- **PMD ICs for telecom / datacom are "time domain" components – why consider frequency domain at all?**

Time Domain		*Frequency Domain*	
Rise / Fall Time	Amplitude	Bandwidth	
Jitter	Gain	Phase Noise	
Overshoot		Return Loss	Group Delay

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Frequency Domain Network Analysis

- Vector network analyzers (VNAs)
- Truly calibrated in-situ measurements at high frequencies (> 1 GHz)
  - Remove all effects of attenuation, dispersion, reflections in cables and test fixtures. Can define and translate reference planes.
  - Very difficult to do in time domain – no commercial instrumentation available (prototype: Agilent LSNA – Large Signal Network Analyzer[1])
- Impedances are naturally handled in freq domain (e.g. Smith chart)
- Limitations for PMD ICs
  - Assumes "linear" time-invariant circuits under small-signal excitation
    - *Digital circuits, limiting / switching drivers are neither . . .*
  - Mapping measured parameters to time domain is often non trivial
    - Bandwidth → rise time, group delay → deterministic jitter, etc.
    - *Not always a useful exercise*

[1] *J. Scott, et al., 2002 IEEE MTT Symposium*

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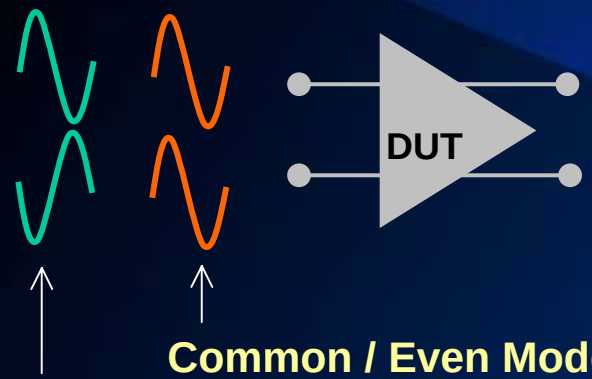
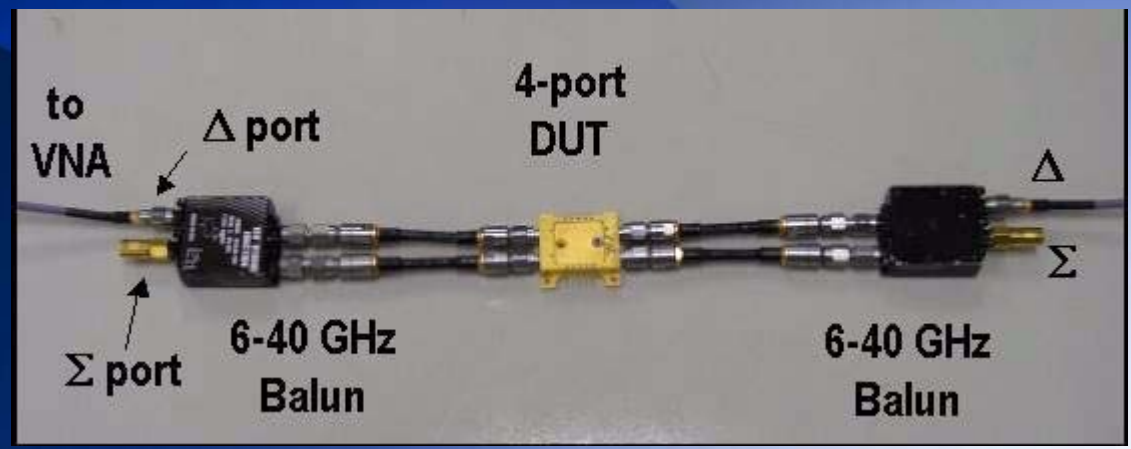
Network Analysis: Differential Circuits

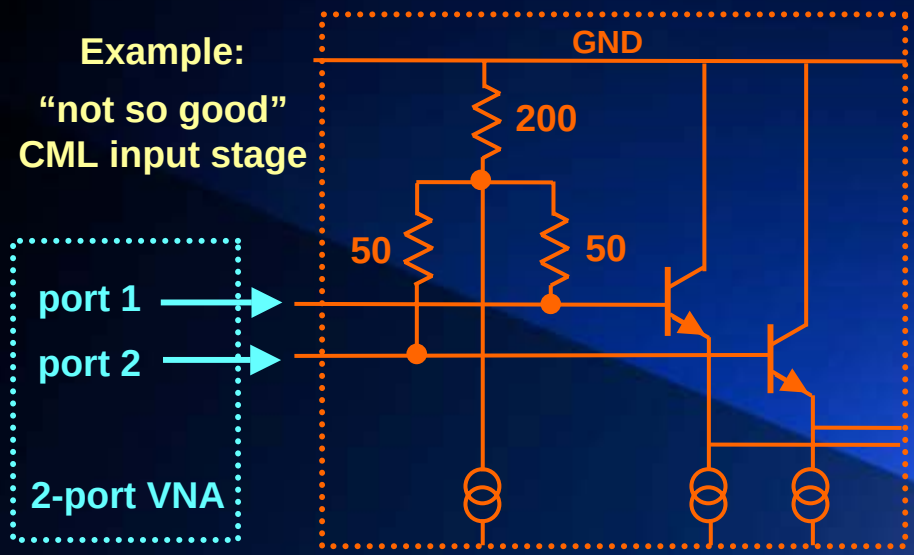
- **Differential PMD integrated circuits**
  - **16 “mixed mode” S-parameters, complete analysis requires 4-port VNA**
  - **Balanced DUT may be measured one mode at a time with 2-port VNA**
    - **Requires 180° hybrid balun**
    - **Band limited – frequency range typically 3 octaves max**
    - **Must fabricate calibration standards – can use TRL**
    - **Mode conversion is not allowed, symmetry is critical**

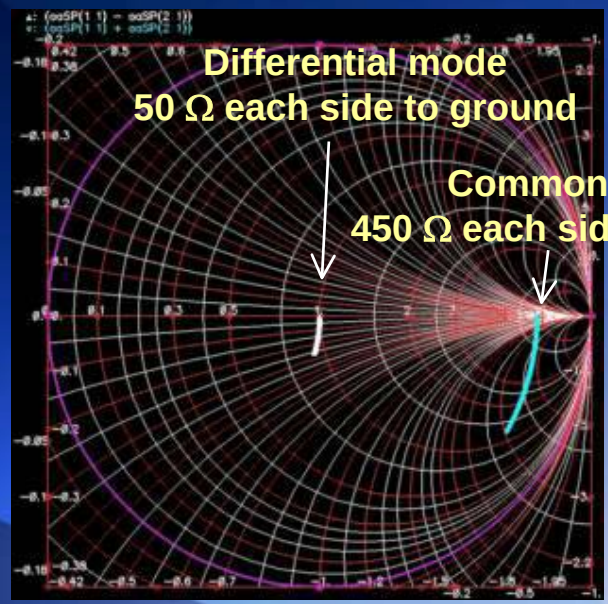




Differential PMD Circuits (con't.)

- **Transmission**
  - Symmetric differential ICs → high common mode rejection (CMR)
  - Measure single-ended gain, add +6 dB for differential output
- **Reflection**
  - Differential & common mode impedances with 2-port VNA technique





$$\Gamma_{DIFF} = \frac{(S_{11} + S_{22}) - (S_{21} + S_{12})}{2} \qquad \Gamma_{CM} = \frac{(S_{11} + S_{22}) + (S_{21} + S_{12})}{2}$$

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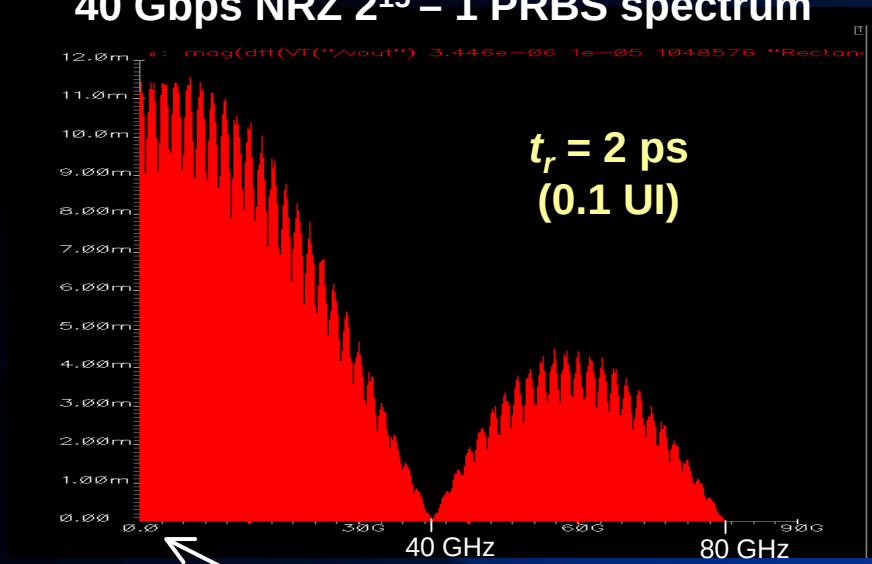
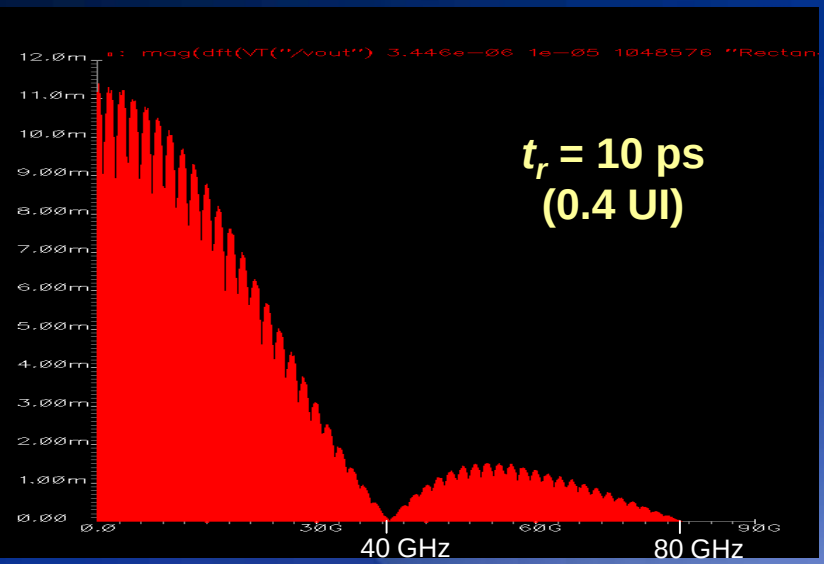
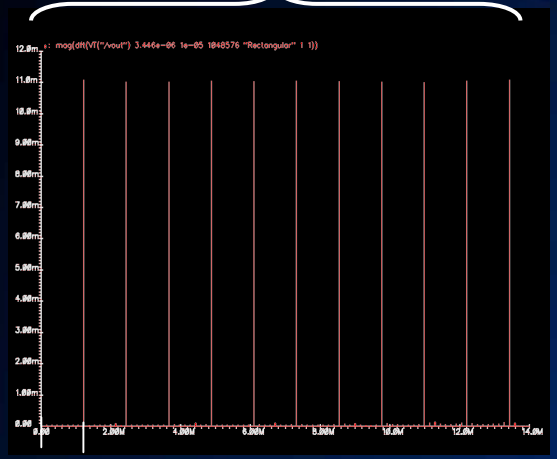
Typical Spectrum of Data Signals in PMD Circuits

40 Gbps NRZ $2^{15} - 1$ PRBS spectrum







Discrete tones related to PRBS sequence length

$$f_n = n\, f_{clk} / (2^m - 1)$$ **or data frame rate**

40 Gbps Data	Lowest Tone
$2^7 - 1$ PRBS	315 MHz
$2^{15} - 1$ PRBS	1.2 MHz
SONET OC-768	8.0 kHz
$2^{31} - 1$ PRBS	18.6 Hz

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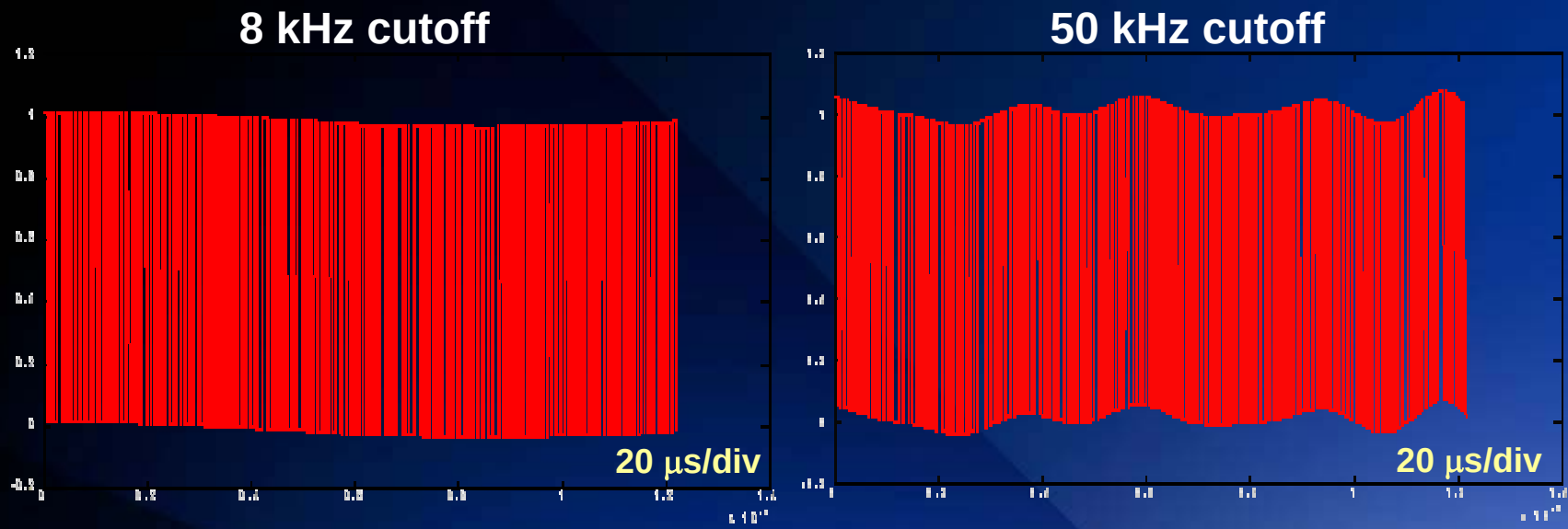
Effect of Low Frequency Cutoff on NRZ Data



- LF cutoff removes lowest discrete tones in data spectrum
  - Causes droop on long consecutive bit runs
  - Another view: “negative tones” added that upset baseline level
  - Baseline ripple occurs at these tone frequencies
- DC blocking capacitors
  - Typically 0.1 μF in 50 Ω system, f_{low} = 16 kHz

→ Cutoff causes deterministic jitter, “fuzz” on eye rails

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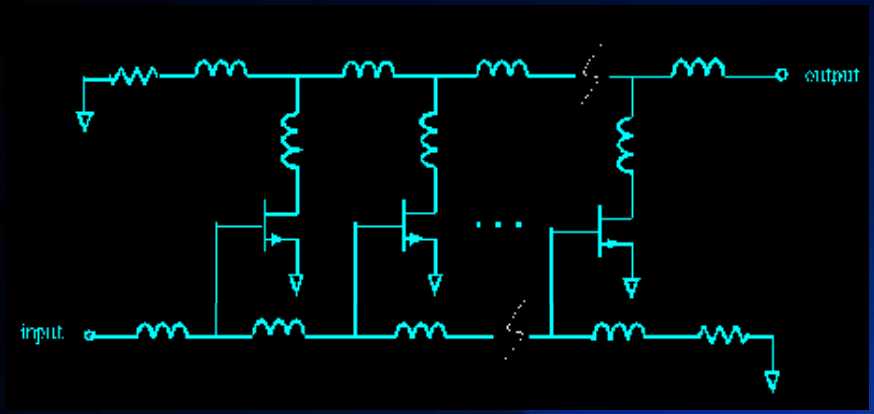
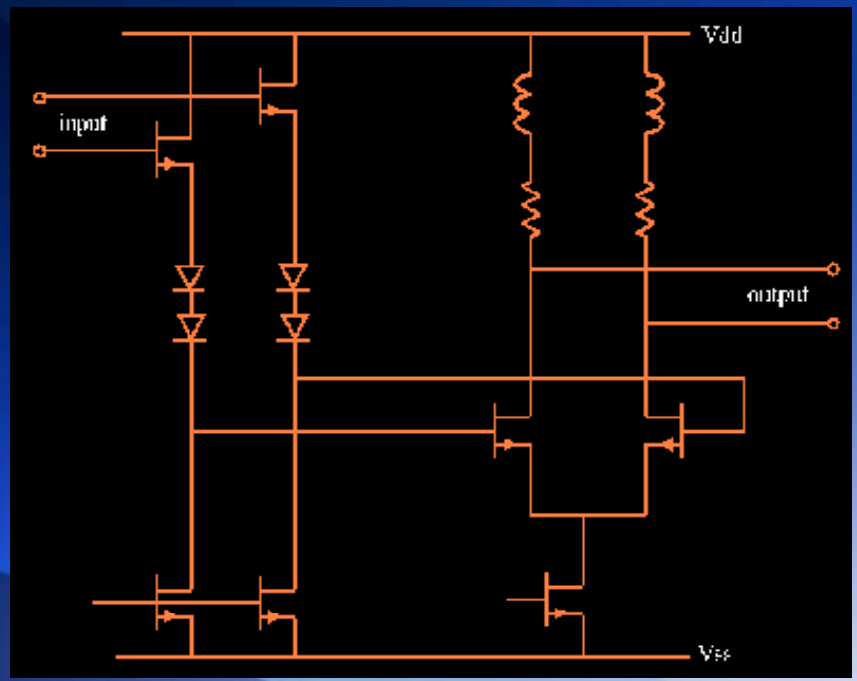
Modulator Drivers / Limiting Amplifiers

- **Two major architectures**
  - **“Microwave” distributed / traveling wave amplifiers (TWAs)**
  - **Switching drivers based on differential pair circuits**





- **Typical VNA measurements**

  Gain (S_{21})
  - Not always measurable or useful

  Return loss (S_{11}, S_{22})
  - Output impedance is time varying in switched circuits

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Bandwidth vs. Rise Time in Linear Circuits

Linear, first-order system with time constant τ

3 dB bandwidth $f_o = \dfrac{1}{2\pi\,\tau}$ **Rise time** $t_r = \tau \ln\left(\dfrac{\text{HI \%}}{\text{LO \%}}\right)$

$$f_o \cdot t_r = \frac{1}{2\pi} \ln\left(\frac{\text{HI \%}}{\text{LO \%}}\right)$$

Bandwidth–rise time product → 350 GHz-ps (10–90%)
→ 220 GHz-ps (20–80%)

→ **Relationship also holds empirically for higher-order systems with damped (monotonic) step response, typ. < 5% error for < 5% overshoot**

Ref: M. S. Ghausi, Principles and Design of Linear Active Circuits, Ch. 16, 1965

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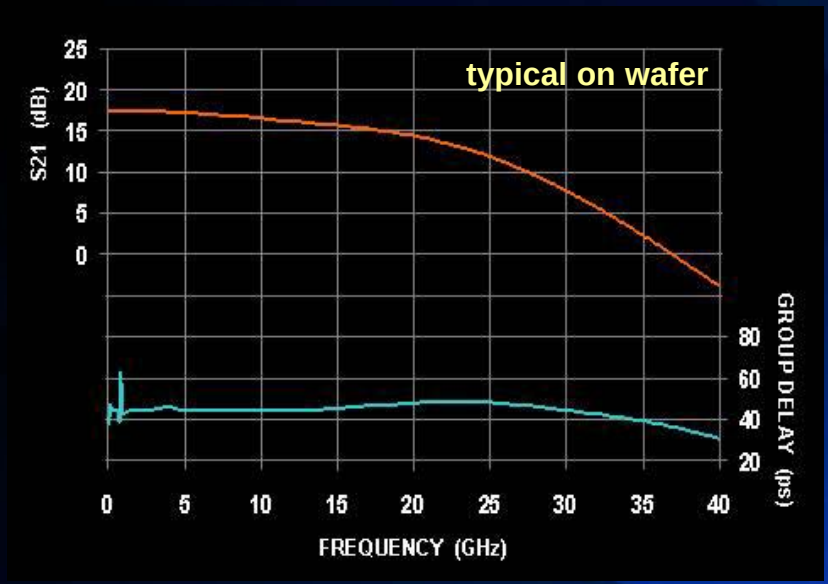
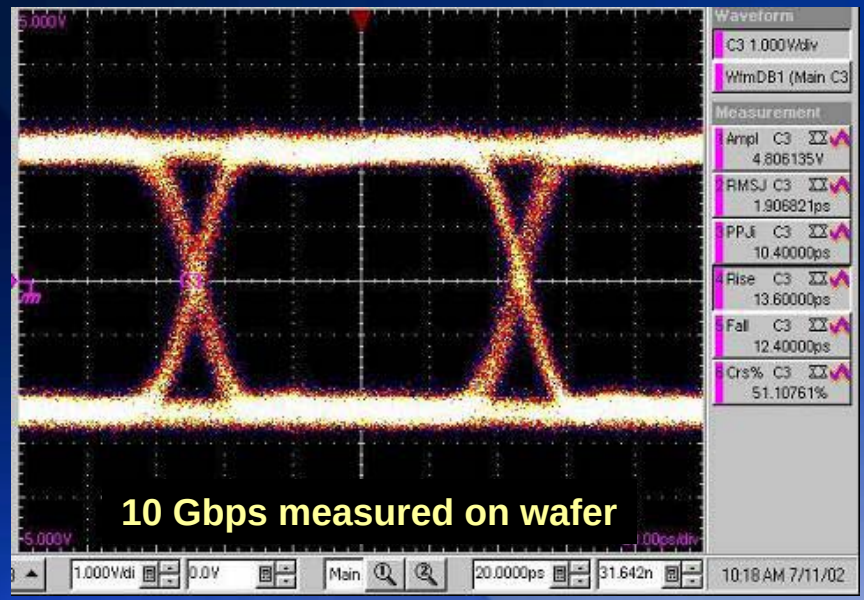
Bandwidth vs. Rise Time: "Quasi Linear" Amplifier

Example: Inphi® 2010DZ Dual MZ Modulator Driver (GaAs pHEMT)





- 18 GHz small-signal $BW_{3\text{-}dB}$
- 12 ps rise time (20–80%)
- Typically 3 dB into compression → weakly limiting
- Bessel-type response / flat group delay → very low jitter

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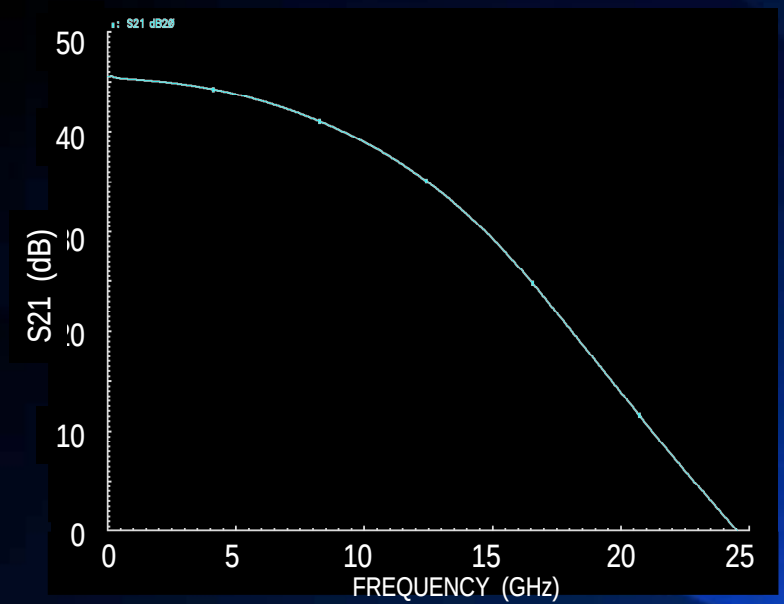
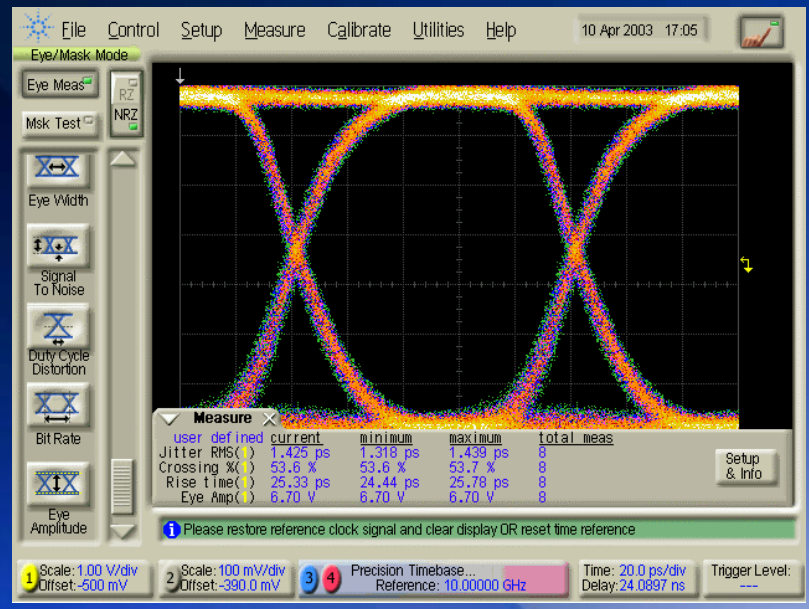
Bandwidth vs. Rise Time: Limiting Amplifier

Example: Inphi® 1310SZ MZ Modulator Driver (InP DHBT)





10 Gbps measured on wafer

6.5 GHz small-signal BW with < 25 ps rise time

- → **Linear estimate 220 GHz-ps / 6.5 GHz = *34 ps !?***
- → ***Operates in a fully switched, nonlinear mode***

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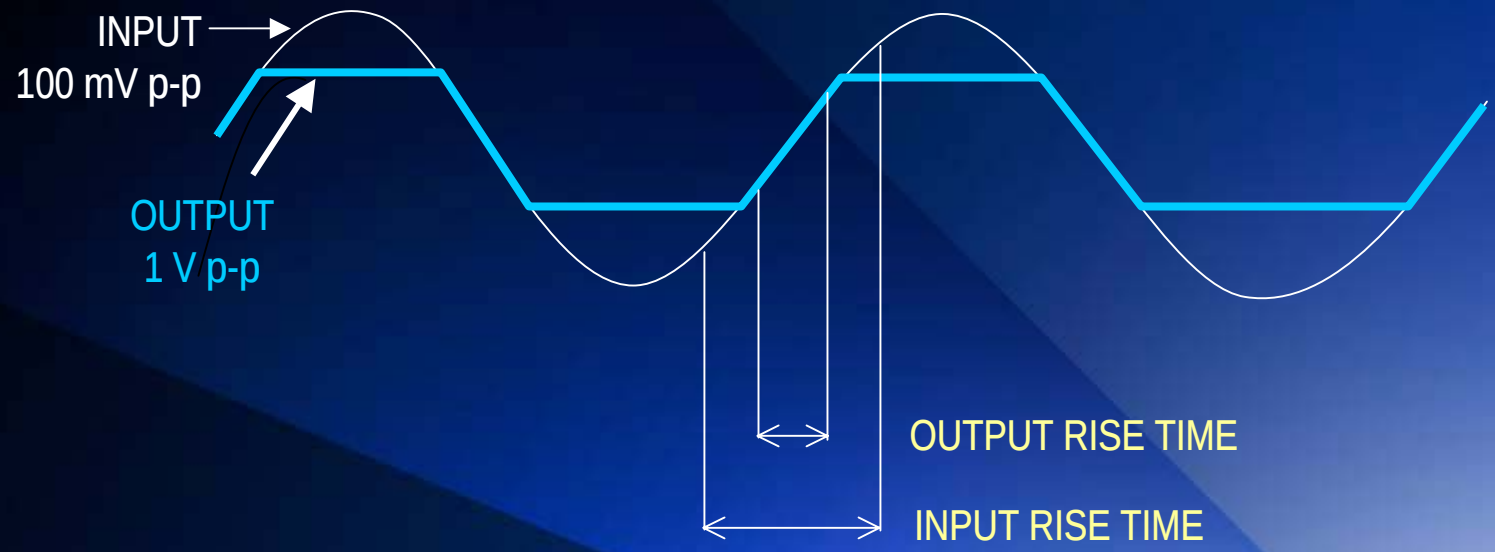
Bandwidth vs. Rise Time in Limiting Amplifiers

Switching / limiting decreases rise time



- Fundamentally nonlinear
- Effective bandwidth increased by harmonic generation

→ Bandwidth–rise time relation falls apart

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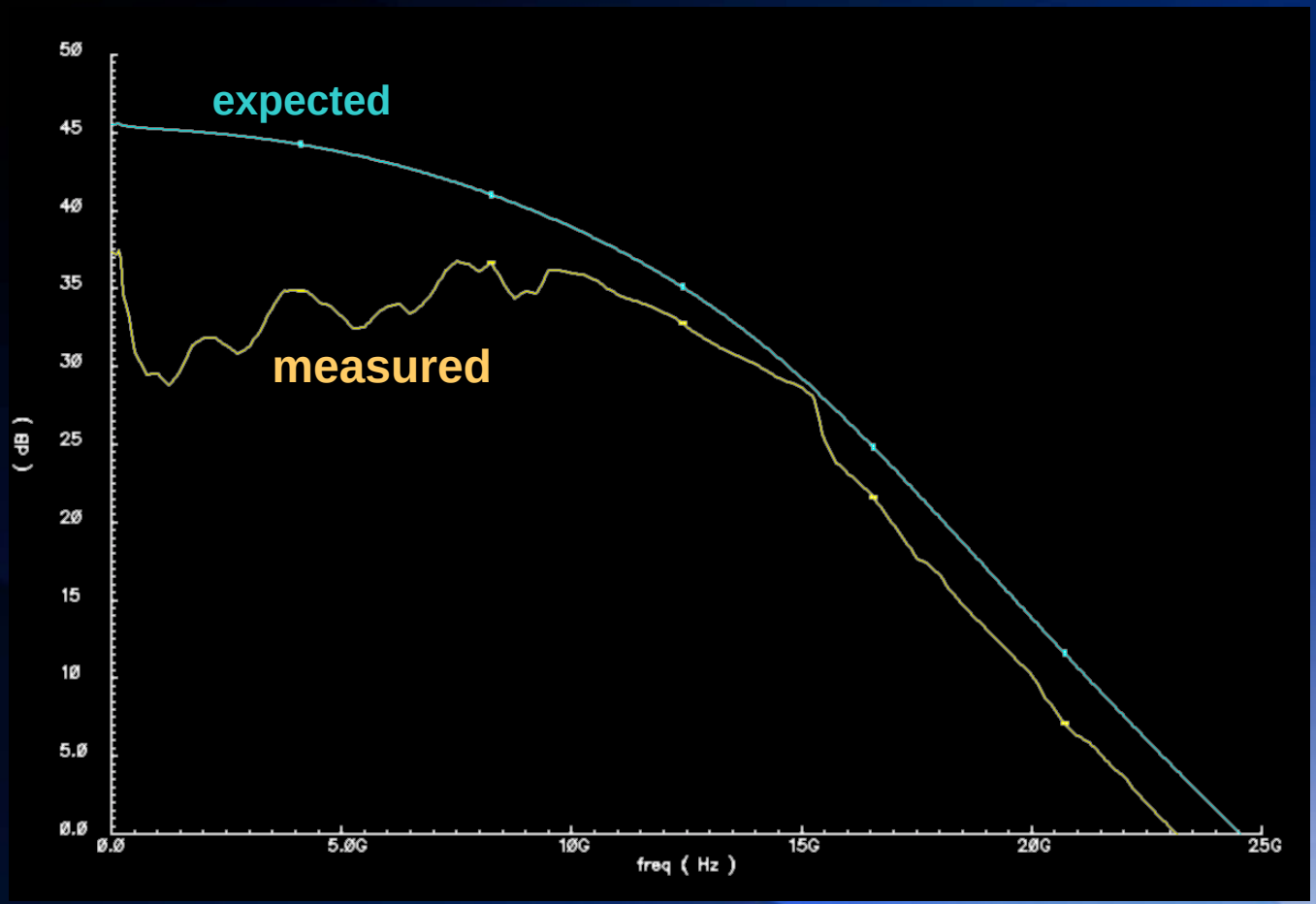
Measuring S_{21} of a Limiting Amplifier = *Trouble*



- Eye diagram, jitter looks fine on an oscilloscope…
- What's going on?

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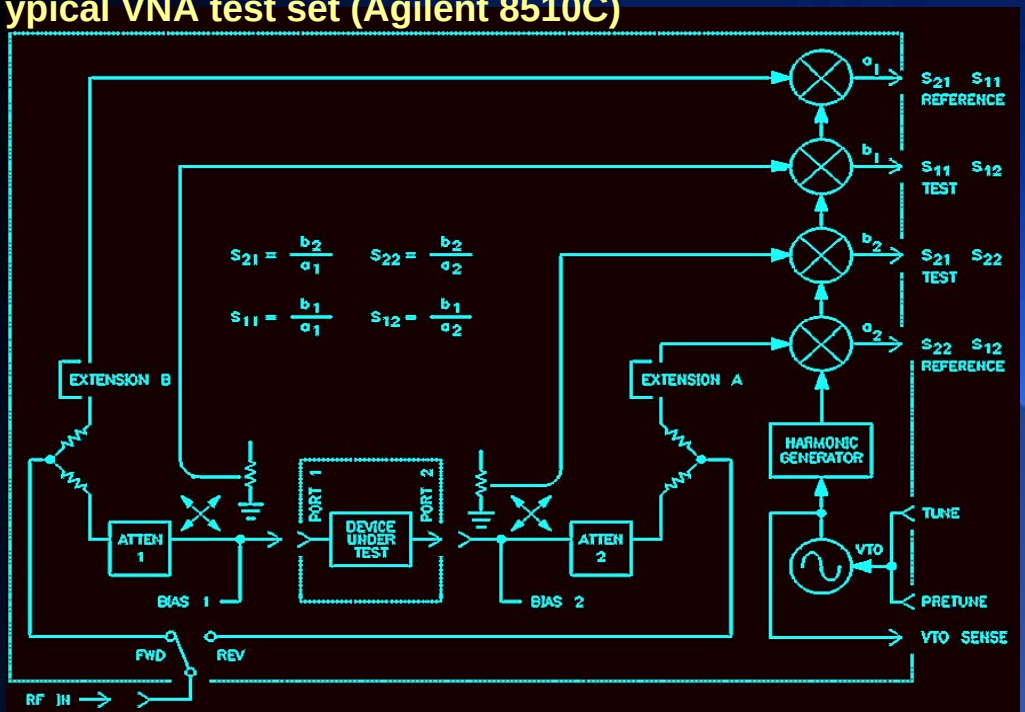
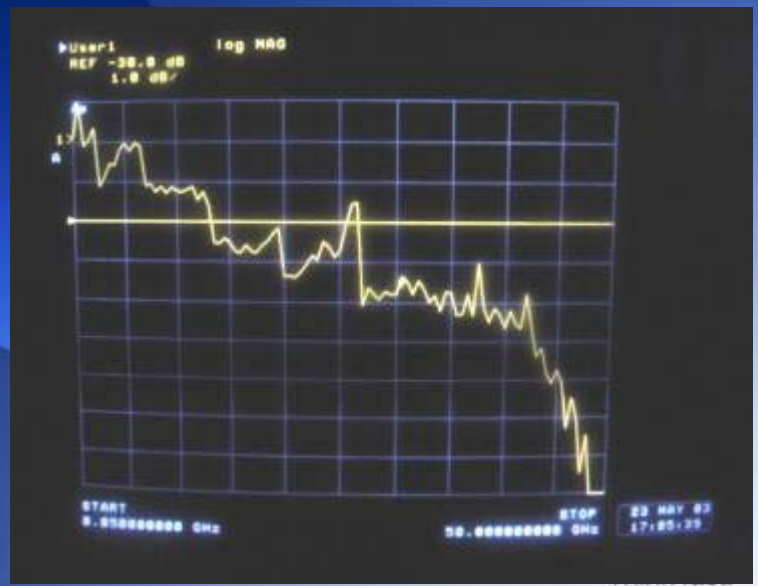
Measuring S_{21} of a Limiting Amplifier

- Limiting fixes b_2 amplitude, ratioed measurement fails
  - Display tracks reciprocal of source power a_1 variation vs. frequency
  - Strange, jagged S_{21} response
  - Usually occurs at low frequency (where source power is highest)
- Measurement is bogus!
  - Need to reduce and/or level VNA source power
  - *Then will data be meaningful? …*

Typical VNA test set (Agilent 8510C)

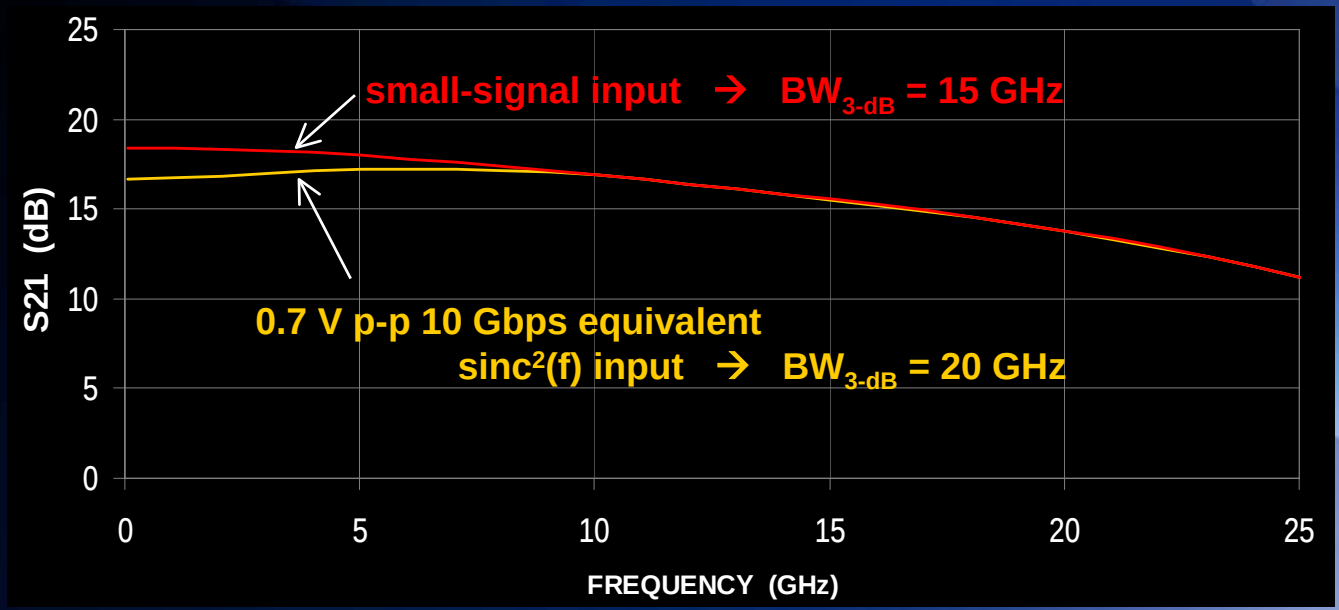


Unleveled source power a_1



Bandwidth of Limiting PMD Amplifier/Driver

- Small-signal S_{21} can be measured on a VNA with low source power
- A "large-signal" S_{21} can be measured with VNA + source leveling
  - Is this useful?
    - Large-signal swept tone is NOT representative of data signal
    - Random NRZ data has $sinc^2(f)$ type power spectral density
    - Data signal compresses amplifier more at low frequencies
    - Effective "data bandwidth" is greater than what VNA will measure
- Rise time is the true measure of speed



Large-signal S-parameter (LSSP) simulation of 10 Gbps driver using Agilent ADS

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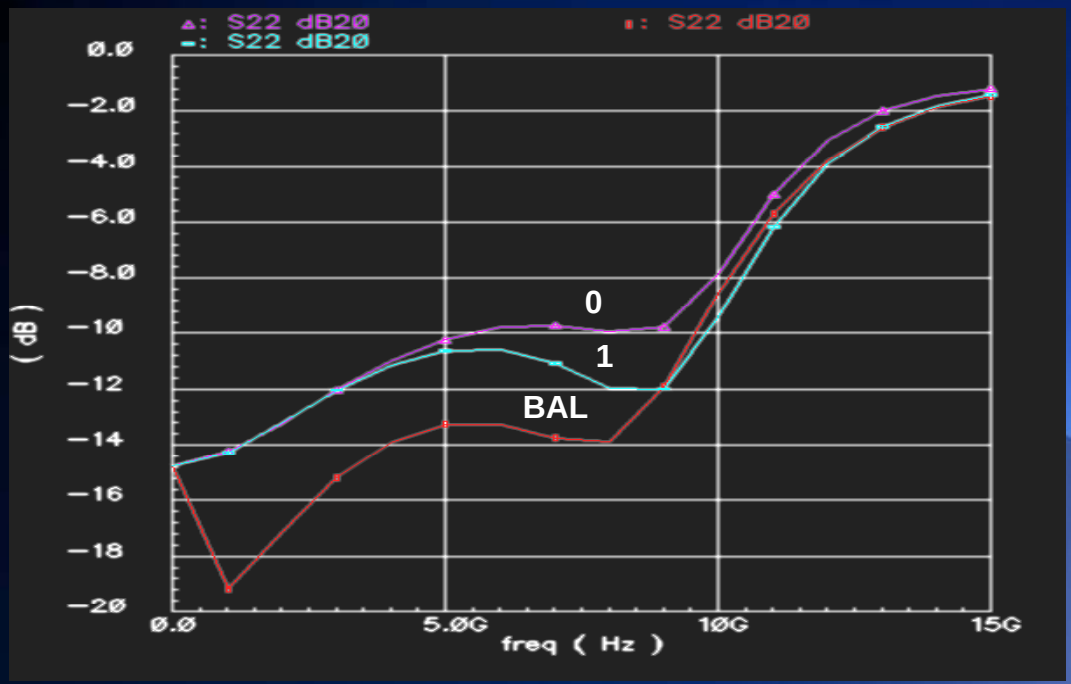
Driver Output Return Loss

- Output impedance is time varying with data signal
- Can measure S_{22} with output state '1' (V_{high}), '0' (V_{low}) or balanced
  - Mostly in '1' or '0' state during operation, but spec sheets show balanced
  - '0' state is typically worst case
    - FET / HEMT driven into triode region (output conductance ↑)
    - Bipolar / HBT driven into quasi-saturation (output capacitance ↑)



Typical output return loss of 10 Gbps switching driver (3 states)

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Conclusions

- Frequency domain measurements for PMD ICs are useful even for time domain circuits
- These measurements provide valuable insight into both single-ended and differential devices
- Be aware of limitations with nonlinear / switching circuits

Presenter Biographies (con't.)

Dr. Carl Pobanz, Principal Design Engineer. Dr. Pobanz is an authority in high-frequency integrated circuit design. At Inphi, he has designed broadband driver ICs for 10 and 40 Gbps optical systems. Throughout his career, Dr. Pobanz has developed HEMT low-noise amplifiers for Ka-band space applications, InP-based LNAs, multipliers, mixers, and power amplifier MMICs for 10–200 GHz systems. Published designs include millimeter-wave IC amplifiers with record high frequency and low noise performance. Dr. Pobanz came to Inphi from Broadcom, where he contributed to the design of 10 Gbps Ethernet SERDES and satellite TV tuner integrated circuits in CMOS. Dr. Pobanz received his B.S., M.S., and Ph.D in electrical engineering from the University of California, Los Angeles.

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