3.4 A 40/50/100Gb/s PAM-4 Ethernet Transceiver in 28nm CMOS

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High-speed signaling using NRZ has approached speeds above 50Gb/s where it is extremely difficult to maintain power efficiency and performance over a wide variety of channels and applications. PAM-4 is emerging as one way to increase throughput in such band-limited channels. Higher modulation formats help to address cost in optical systems by packing more bits/wavelength [1]. Strong momentum in standards to adopt PAM-4 reflects these significant trends in the industry. At the same time, migrating transceiver designs to current technology nodes have narrowed the power gap between traditional Analog and ADC-DFE-DAC-based systems for high-speed applications. These factors make ADC-based receivers a highly desirable choice, as is also the trend in wireless communications.

The transceiver shown in Fig. 3.4.1 is built to support a wide range of Ethernet applications. The block diagram of the complete receiver is shown in Fig. 3.4.2. A merged equalizer-VGA (Fig. 3.4.2b) performs coarse equalization and drives the T/H circuits, minimizing the number of stages. The VGA has a gain range >12dB in 0.1dB steps and a BW >136GHz. A high-frequency gain-boost of up to 8dB provides system SNR improvement in high loss channels. This equalizer-VGA achieves SNR >41.7dB and THD >36dB over all gain, boost and process corners by employing $g_{m}$-boosted source degeneration [2]. $g_{m}$ of transistors P1 and P2 is boosted by the loops created by N1, N3, N7 and N2, N4, N8, respectively. Programmable gain is achieved through differentially modulating the mirrored transconductance gain by creating a differential $V_{ds}$ bias on N3, N5 and N4, N6. Each VGA drives 4 T/H switches operating at 3.5GHz/s each. A unity-gain buffer is used at the output of each track-and-hold to drive four sample-and-hold circuits and their associated capacitive DACs. A feed-forward-based negative $g_{m}$ technique in an otherwise conventional source follower helps to optimize signal-to-noise performance and linearity at low supply voltages. A replica circuit controls the negative-$g_{m}$ in the buffers ensuring constant gain over process, voltage, and temperature. Each of the 32 sub-ADCs is a SAR core clocked at 75GHz.

Independent reference buffers minimize non-linear and signal dependent noise coupling between channels.

The DSP core (Fig. 3.4.3) performs the calibration for offset, gain, timing skew estimation and correction of the analog front-end. The DSP core employs a set of parallel FFEs for channel equalization. The parallel factor was chosen to be a multiple of the number of sub-ADC channels to optimize power consumption. The gain of the 32 time-interleaved channels is estimated using an envelope detector. Any gain mismatch is compensated by adjusting the associated reference voltage, which maximizes range of each ADC slice. Residual gain errors are further corrected in the DSP. Offsets of each interleaved channel are estimated digitally by computing the average of the slicer error at the FFE output that corresponds to each signal path and corrected inside the DSP core. Here, we trade-off dynamic range of the ADC for offset correction to avoid DACs in the signal path that degrade bandwidth. Timing mismatch is estimated digitally by using correlated properties of the pin input signal. Digital controls are fed back to small delay cells that alter the sampling phase of the $8/7$ T/H clocks with a resolution of ~100fs.

Figure 3.4.3 plots SNDR of the entire receive channel and the impact from timing calibration. BW mismatch between the different AFE paths is compensated by independent adaptation of the FFE slices.

The DSP employs an adaptive PAM-4 DFE. The feedback taps are limited to one tap to minimize impact of error propagation. Baud rate clock recovery is used which is based on the well-known Mueller-Muller timing recovery scheme [3] but taking inputs directly at the ADC output, thus eliminating interaction problems with FFE-DFE adaptation while providing a low latency clock recovery path. A measured jitter tolerance plot for NRZ modulation is shown in Fig. 3.4.3 against a VSR mask. The clock recovery scheme can be made truly reference-less by taking advantage of the reference-less HOST VSR link. The recovered clock is filtered prior to ADC sampling. This allows the reference to be powered down.

A DFL, as shown in Fig. 3.4.4a, generates the timing phases for the ADC from a 7GHz clock from the PLL. Static phase offset (SPO) is a well-known problem in DFLs. A differential quadrature phase detector achieves the goal of low SPO, allowing for healthy timing margins in the ADC clocking and easing start up of the DSP engine.

The line transmitters can be configured as two PAM or four NRZ links. The latter provides support for segmented modulators that generate PAM-4 in the optical domain. The transmitter implementation, shown in Fig. 3.4.5a, is a traditional CML implementation with shunt peaking in the final stage. The driver provides swing levels up to 1.4Vpp and incorporates a 3-Tap FIR filter with independent control on the MSB and LSB paths. The MSB to LSB ratio can also be altered to provide pre-distortion on the PAM-4 eye, which is useful in applications where the PAM transmitter interfaces with optical drivers. Figure 3.4.5 shows the transmit eye diagrams measured at the chip balls.

A skew control mechanism shown in Fig. 3.4.5b, auto-zeroes electrical and logical skew in NRZ mode. It can also pre-compensate skews (< ±1UI) that occur downstream. An analog phase detector senses the skew and a FSM corrects for it by adjusting the offset in the PLL charge-pump. A delta-sigma modulator driving this offset current provides very fine control of the PLL phase (resolution <100fs).

The FSM also calibrates the loop to be able to introduce any required skew and maintain it over operating conditions. The noise introduced by the offset delta sigma is negligible. The entire system shows a simulated 3σ error of < +/-0.5ps peak-to-peak due to random mismatches.

A fractional-N PLL provides the required clocks for the TX and RX paths and is shown in Fig. 3.4.6. The VCO is inductor-based with dual tuning paths (9.9 to 15.5GHz). A simple amplifier and RC filter form a slow path that drives Vctrl, fast close to a target voltage. This has several advantages: maximizing charge pump headroom and linearity, stabilizing the fast loop $K_{	ext{u}}$ over tuning range, tracking temperature and reducing the loop filter size. The multi-modulus (MM) divider is based on Vaucher’s extended range topology. This implementation enables transition across stage boundaries, smoothly overcoming a key limitation in the original topology. Figure 3.4.6 shows integrated rms jitter of 11fs on the TX outputs in a frequency band from 1kHz to 100MHz.

Power supply noise management is a key aspect of high performance communication links. Both PSRR and random noise from regulators impact overall SNR of the analog front-ends. The regulator topology shown in Fig. 3.4.6 uses feed-forward injection. The frequency of injection is tuned to attenuate external switching regulator noise, which can often occur around PLL corner frequencies. This attenuation allows for reduced on-board filtering requirements. Source degeneration is employed in the error amplifier to further reduce 1/f noise contributions. The chip is fabricated in 28nm CMOS. The chip consumes 2.4W with 100G traffic and 25Gbaud PAM-4 on the line while the DSP was set to 10-tap FFE configuration.

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References:
Figure 3.4.1: Transceiver Block diagram.

Figure 3.4.2: RX and equalizer-Vga.

Figure 3.4.3: DSP Block diagram.

Figure 3.4.4: DLL and Regulator.

Figure 3.4.5: TX Block diagram.

Figure 3.4.6: PLL block diagram.
Figure 3.4.7: Die Photo and Performance summary.