Implementing A High-Speed Differential Encoder

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Introduction

Differential encoding of data is required for some modulation schemes such as duobinary and differential phase shift keying. Both these modulation schemes are now being considered for optical links at high data rates such as 10 Gbps and 40 Gbps. This paper describes how a differential encoder can be implemented using high-speed logic parts from Inphi.

Differential Encoding

Let d_k be a sequence of binary bits that are the input to a differential encoder and let c_k be the output of the differential encoder. Then

$$c_k = c_{k-1} \oplus d_k \quad (\oplus \text{ is modulo 2 addition}) \tag{1.1}$$

The most direct implementation of the above equation is to use an exclusive-OR (XOR) gate with a delay in the feedback path as follows:

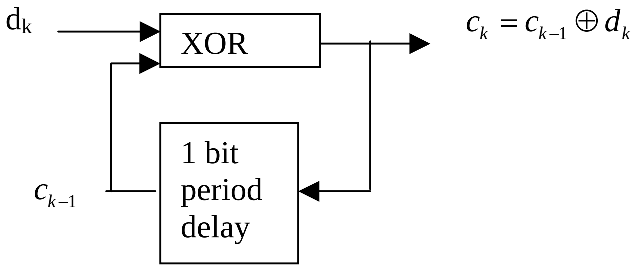


Figure 1. Differential encoder implementation using a XOR gate

However, implementing the 1 bit period delay (1 bit period = 25 psec at 40 Gbps) in the feedback path can be difficult when working with discrete components. A feed-forward circuit without such critical delays is a more practical circuit. One such implementation is shown in Figure 2.

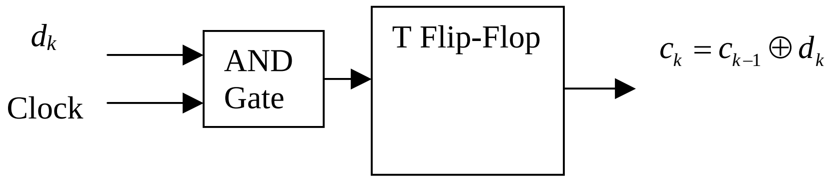


Figure 2. Differential encoder implementation using an AND gate and T flip-flop

In the above circuit, the data bit d_k gates the clock, i.e., when $d_k = 1$ the clock is transmitted through the AND gate, and when $d_k = 0$ the clock is not transmitted through the AND gate. Thus when $d_k = 1$ the T flip-flop output changes state (which is the same as adding 1 modulo 2 to the T flip-flop output), and when $d_k = 0$ the T flip-flop output does not change state (which is the same as adding 0 modulo 2 to the T flip-flop output). Thus feedback paths with any critical delays have been eliminated. However, the gated clock pulses at the output of the AND gate have a duration of half the bit period (12.5 psec in the case of 40 Gbps), which requires that the logic parts have sufficient bandwidth to handle such high-speed signals. (For implementing such an encoder at 10 Gbps, the 25 Gbps logic parts from Inphi are recommended.) This implementation also requires that the clock and data signal to the AND gate be aligned such that the rising clock edge should lie in the middle of a data bit:

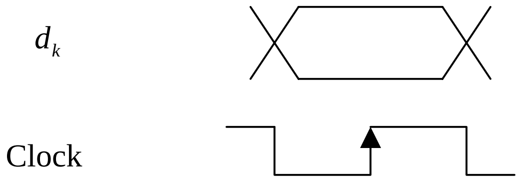
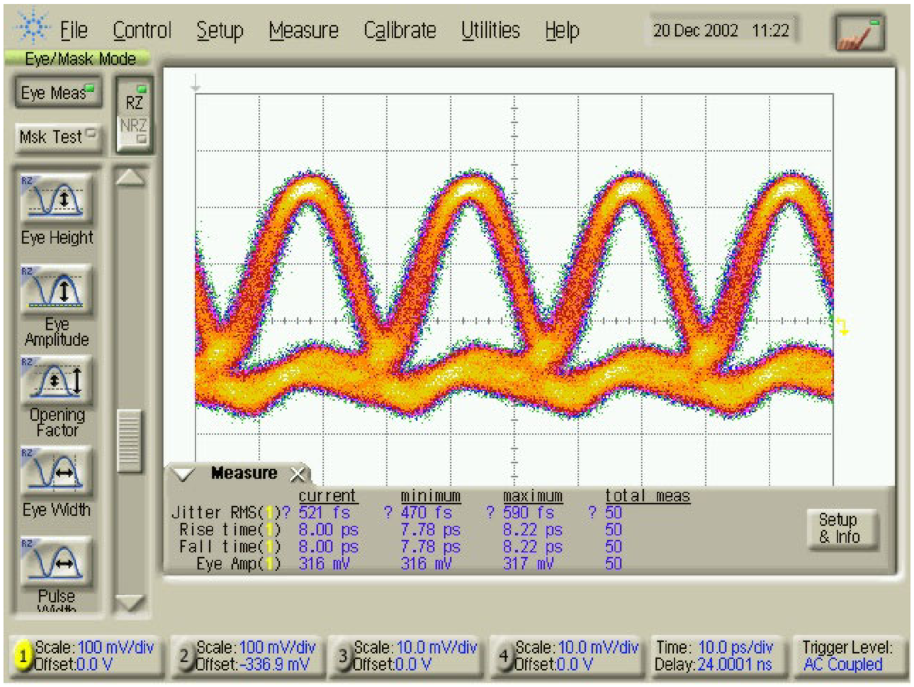


Figure 3. Alignment of data and clock

Implementation and Results

The circuit in Figure 2 was implemented using the Inphi® 50713OR and 50721TF logic parts (these are positive supply parts, but negative supply parts are also available). While the 50713OR gate is labeled as an OR gate, the gate can be used to implement an AND gate by simply inverting its inputs and output {not[not(x) or not(y)] = (x and y) by DeMorgan's law}. Since all signals are differential, the signal can be inverted simply by reversing the wires when connecting the parts (for a more detailed explanation, please refer to the data sheet and the application note for these parts). A positive supply voltage of 3.3 V was used.

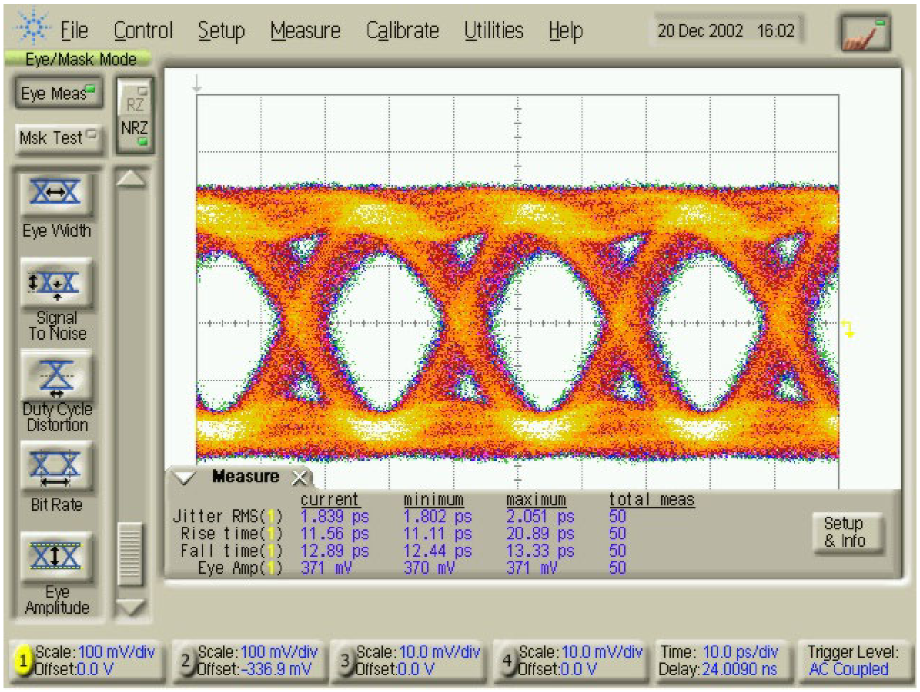
The eye diagram signal at the output of the AND gate is shown in Figure 4 for a 40 Gbps, 2^15 –1 PRBS input. Note that only the positive parts of the clock signal are gated through, resulting in a 40 Gbps RZ signal. The output of the toggle flip-flop is shown in Figure 5 as a 40 Gbps NRZ signal. The output amplitude and jitter are somewhat compromised by finite cable lengths.



```
                 current      minimum      maximum      total meas
Jitter RMS(1)? 521 fs     ? 470 fs     ? 590 fs     ? 50
 Rise time(1)  8.00 ps      7.78 ps      8.22 ps      50
 Fall time(1)  8.00 ps      7.78 ps      8.22 ps      50
   Eye Amp(1)  316 mV       316 mV       317 mV       50
```

1 Scale: 100 mV/div Offset: 0.0 V
2 Scale: 100 mV/div Offset: -336.9 mV
3 Scale: 10.0 mV/div Offset: 0.0 V
4 Scale: 10.0 mV/div Offset: 0.0 V
Time: 10.0 ps/div Delay: 24.0001 ns
Trigger Level: AC Coupled

Figure 4. Output of AND gate at 40 Gbps, 2^15-1 PRBS sequence



```
                 current      minimum      maximum      total meas
Jitter RMS(1)  1.839 ps     1.802 ps     2.051 ps     50
 Rise time(1)  11.56 ps     11.11 ps     20.89 ps     50
 Fall time(1)  12.89 ps     12.44 ps     13.33 ps     50
   Eye Amp(1)  371 mV       370 mV       371 mV       50
```

1 Scale: 100 mV/div Offset: 0.0 V
2 Scale: 100 mV/div Offset: -336.9 mV
3 Scale: 10.0 mV/div Offset: 0.0 V
4 Scale: 10.0 mV/div Offset: 0.0 V
Time: 10.0 ps/div Delay: 24.0090 ns
Trigger Level: AC Coupled

Figure 5. Output of T flip-flop at 40 Gbps, 2^15-1 PRBS sequence

To verify that the output signal is indeed the differentially encoded version of the input bit stream, the output signal was run into a bit error rate tester (BERT).

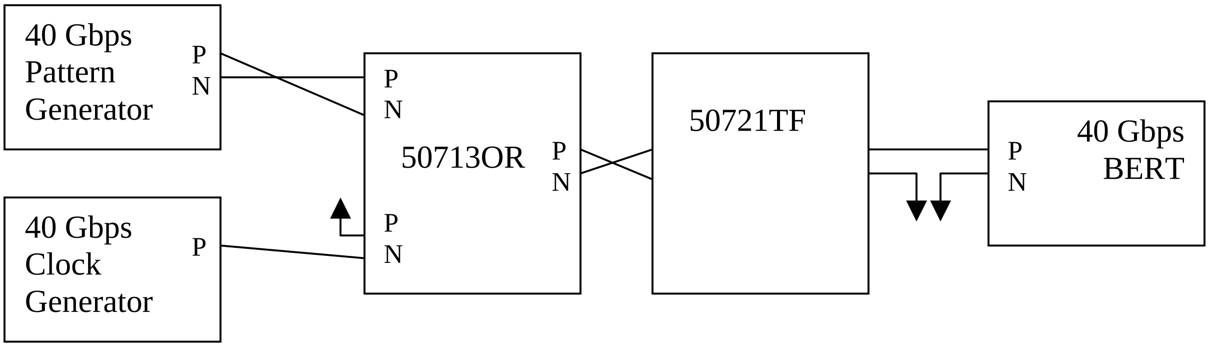


Figure 6. Bit Error Rate Test

An interesting property of the 2^{15}-1 PRBS sequence generated by the pattern generator (generator polynomial = $1 + x^{14} + x^{15}$) is that after differential encoding, it is the same PRBS sequence shifted by 14 bits. [This property that a differentially encoded PRBS sequence is a delayed version of the original sequence holds true whenever the generator polynomial is of the form $1 + x^{n-1} + x^{n}$, $n > 0$, and the delay between the PRBS sequence and the differentially encoded sequence is (n-1). For a proof see the appendix below.] Since the BERT is capable of aligning the transmitted and received data streams, the delay is of no consequence when measuring the BER. It was verified that a BER of 0 was obtained for the 2^{15}-1 PRBS sequence and the 2^{7}-1 PRBS sequence (generator polynomial = $1 + x^{6} + x^{7}$).

Conclusion

Differential encoding can be successfully implemented using discrete logic parts at data rates as high as 40 Gbps. These parts are ready for deployment in high-speed optical communication systems that use duobinary or differential phase shift keying modulation. Positive and negative supply parts are available for this purpose.

Acknowledgements

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Appendix 1

The below proof shows that a differentially encoded PRBS sequence c_k , is a delayed version of the original sequence d_k , whenever the generator polynomial is of the form $1+x^{n-1} + x^{n}$, n > 0, and the delay between the PRBS sequence and the differentially encoded sequence is (n-1).

By definition

$$d_k = d_{k-(n-1)} \oplus d_{k-n} \tag{1.2}$$

We need to verify that the sequence c_k given by equation (1.1) satisfies the property

$$c_k = d_{k-(n-1)} \tag{1.3}$$

Substituting (1.3) into (1.1) we get

$$d_{k-(n-1)} = d_{k-n} \oplus d_k \tag{1.4}$$

Since modulo 2 subtraction is the same as modulo 2 addition, we see that (1.4) is the same as (1.2) and thus the result is true.