

Jitter Measurements for ≥ 10 Gbps PMD ICs

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Overview

- **Equipment limitations at ≥ 10 Gbps**
- **Jitter basics**
 - Jitter spec in data sheets
 - Jitter components
 - Jitter and scope eyes
- **Measuring random jitter**
- **Measuring deterministic jitter**
 - Shortcut
 - Edge-by-edge method
 - DCD
 - Example
- **Summary**

Equipment Limitations at ≥ 10 Gbps

- **Advanced jitter analysis equipment not available at present**
 - Lack of sufficiently fast real-time sampling scopes (roughly ≥ 40 Gbps would be needed)
- **50–70 GHz equivalent time sampling scope (DCA) readily available – let's try to use that...**
- **Equipment impacts measurement accuracy – use the best you have**

Jitter Spec in Data Sheets

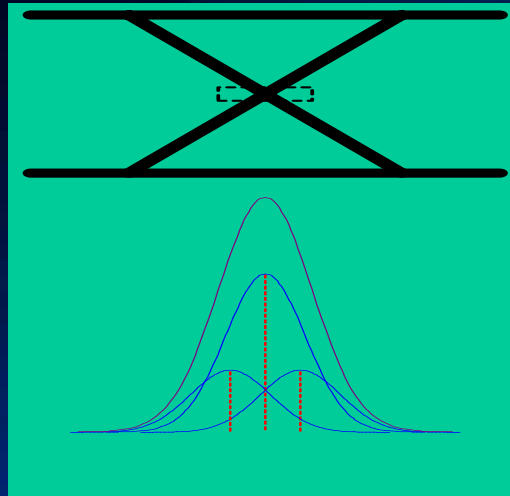
- **Added jitter** is key parameter for PMD ICs
 - **Some spec total output jitter**
 - ◆ Only valid if you have a jitter-free input (a clocked driver is close)
 - **Must be separated into random jitter (RJ) and deterministic jitter (DJ) components to correctly predict system margins**
 - **Pattern must be stated for DJ spec**

Jitter Components

- **Random jitter (RJ)**
 - Unbounded value, rms “unit”
 - Thermal noise, shot noise
- **Deterministic jitter (DJ)**
 - Has a pattern-dependent probability density
 - Bounded value, peak-to-peak “unit”
 - Intersymbol interference (ISI), coupling, duty cycle distortion (DCD), supply noise
- **Some deterministic jitter can look random depending on the measurement technique used (e.g. DJ uncorrelated to trigger)**

Jitter & Scope Eyes

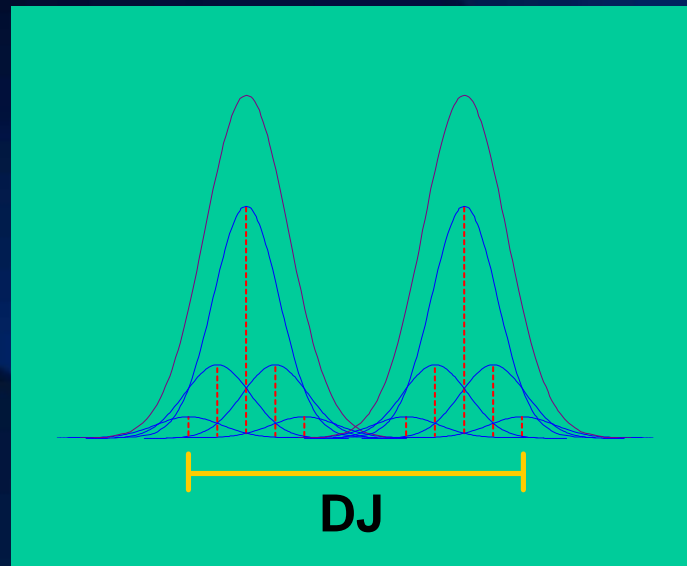
- “Jitter” is convolution of DJ and RJ components



- DJ also has a probability density (though bound)
- DJ often buried in a pseudo-Gaussian distribution (no distinct double peaks)
 - No double peaks does *NOT* mean no DJ!

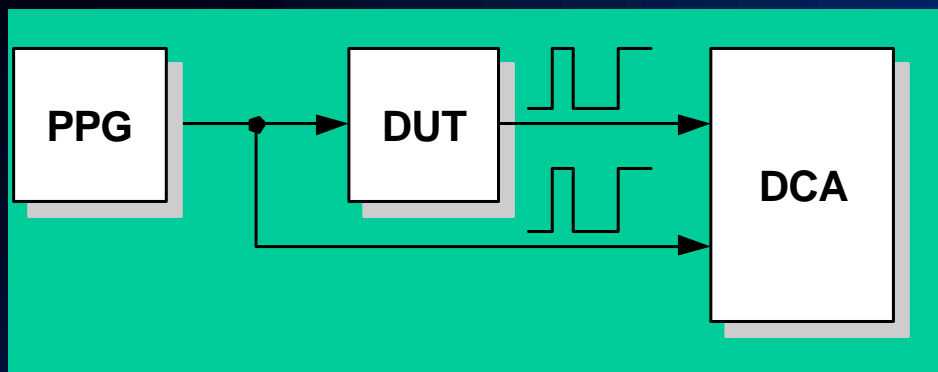
Jitter & Scope Eyes (con't.)

- Why DJ generally isn't the distance between the peaks



- DJ extends beyond peaks!

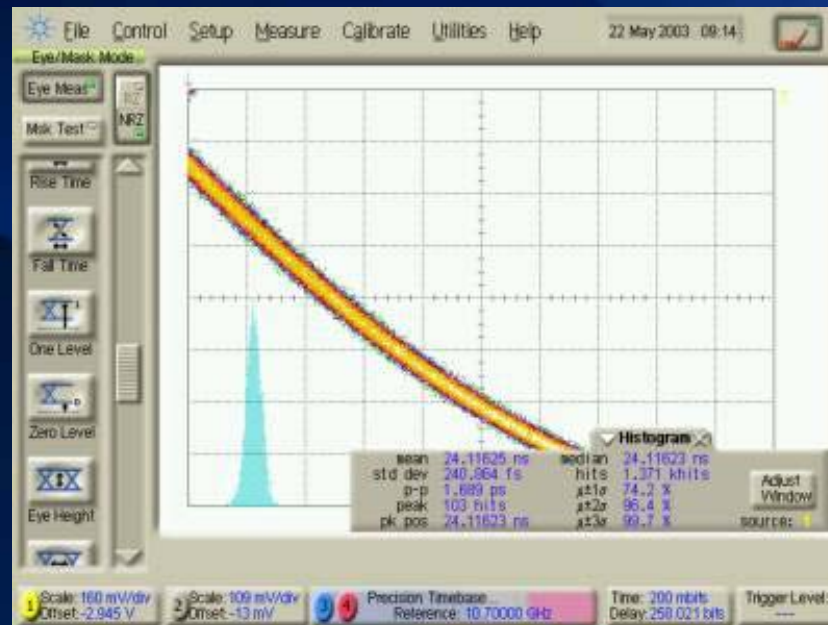
Measuring Added Jitter Using DCA



- Measure DUT output as well as input
 - Eliminates source / setup DJ and potential DCA time base wander problem
 - Use a low jitter input whenever possible in order to get accurate added jitter numbers
 - Clocked DUTs: measure CLK instead of DUT input data

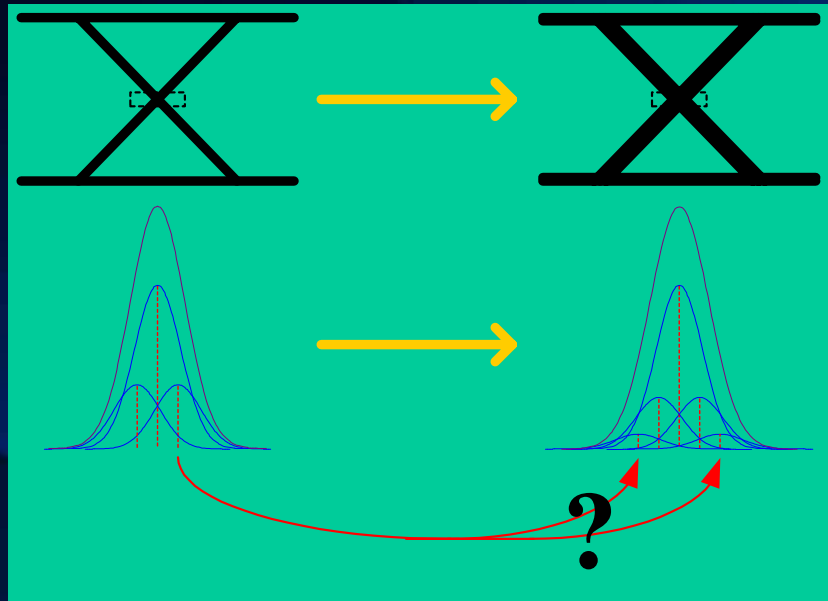
Added Random Jitter

- 1010 pattern, trigger on either edge
- Measure rms value: $RJ_{DUT} = \sqrt{RJ_{OUT}^2 - RJ_{IN}^2}$
- Triggering on one edge prevents DCD effects



Added Deterministic Jitter

- DJ transfer input \rightarrow output is unknown

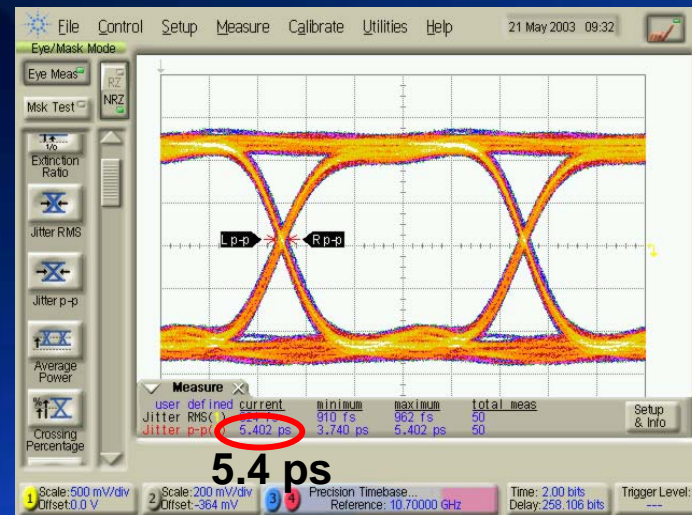
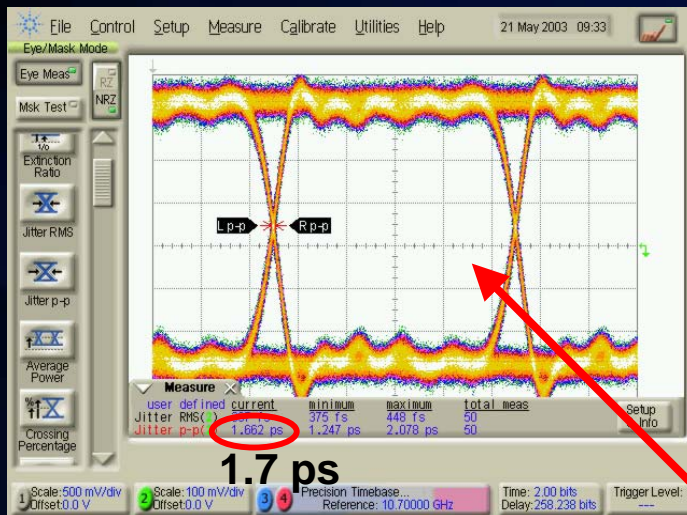


- Thus one *cannot* assume that

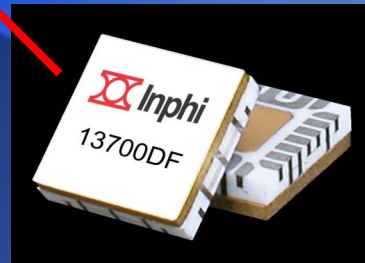
$$DJ_{DUT} = DJ_{OUT} - DJ_{IN}$$

Estimating DJ

- Bounds on added DJ can be found from input and output eyes alone (sum and difference are extremes)
- Measure input and output DJ (eye mode, few samples to avoid outer RJ tails in result, peak-to-peak measurement)

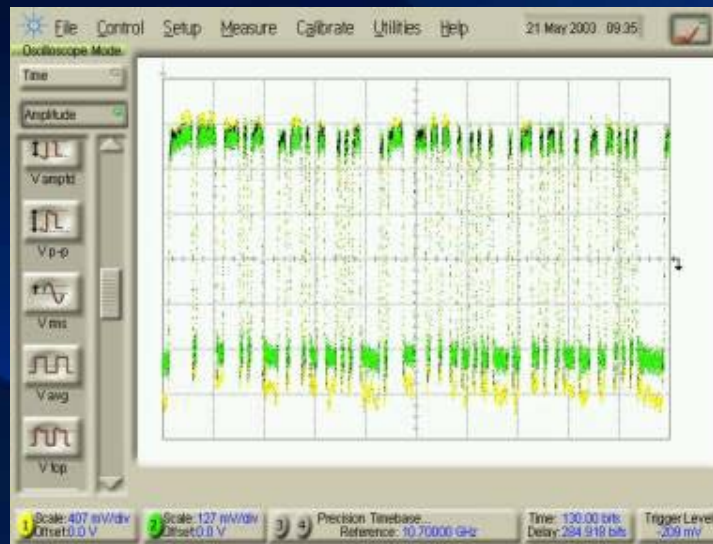


- Above example results in $3.7 \text{ ps} \leq \text{DJ} \leq 7.1 \text{ ps}$ (a *clean* input is important here)
- This method does *not* yield the exact added DJ value!



Edge-by-Edge Method

- Pattern trigger, use averaging (more is better), max horizontal resolution (e.g. Maxim app note)
- Measure *bit-aligned* input & output simultaneously to eliminate DCA time base wander



Problem: DCA accuracy with large time span

– $2^7 - 1$ @ 10 Gbps, 4050 points → 3 ps resolution

Edge-by-Edge Method (con't.)

- Walk through entire pattern in high time resolution mode, e.g. 2 bits span → 100 fs resolution



Problems

- Very time consuming when averaging
- Limits pattern length to < 1000 bits in reality

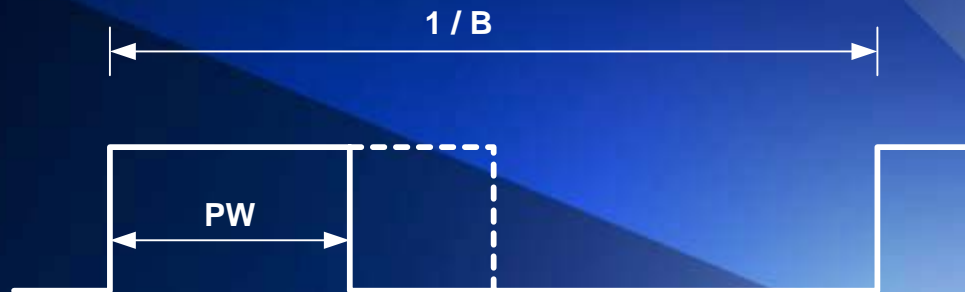
Edge-by-Edge Method (con't.)

- Measure delay between all falling input / output edge pairs – define $\Delta_{\text{fall}} = \text{tpdf}_{\text{max}} - \text{tpdf}_{\text{min}}$
- Measure delay between all rising input / output edge pairs – define $\Delta_{\text{rise}} = \text{tpdr}_{\text{max}} - \text{tpdr}_{\text{min}}$
- $\text{DJ}_{\text{pp}} = \max \{ \Delta_{\text{fall}}, \Delta_{\text{rise}} \}$
- Method does *not* include DCD in DJ number
 - This automatically separates DCD from correlated DJ
- Uncorrelated DJ not captured

DCD Method

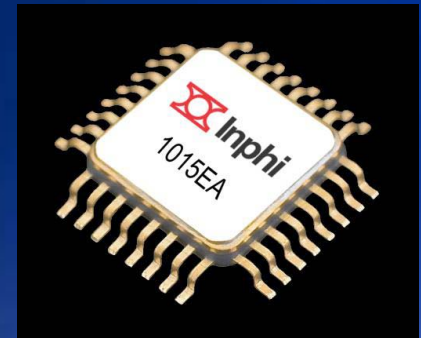
- 1010 pattern, trigger on either edge
- Averaging on (eliminates RJ & uncorrelated DJ)
- Measure narrow pulse width
- Calculate peak-to-peak jitter by

$$DJ_{DCD, pp} = 1/B - PW$$



Example: 1015EA Electro-Absorption Driver

- PRBS $2^7 - 1$ @ 10.7 Gbps, 4050 points
- Added RJ = 240 fs rms
- Added DJ outer bounds:
 $3.7 \text{ ps} \leq \text{DJ} \leq 7.1 \text{ ps}$
- Added DJ – accurate measurement
 - DJ = 5.4 ps with averaging = 16 (time 5 min)
 - DJ = 4.6 ps with averaging = 64 (time 20 min)



Conclusions

- For 10 Gbps and beyond, measuring *added* deterministic jitter *accurately* is difficult but important
- High accuracy is time consuming and not well suited for production test
- With a *very clean* input, the outer bounds of added DJ can be estimated quickly with reasonable accuracy

Presenter Biographies (con't.)

Dr. Steffen Nielsen, Principal Design Engineer. Dr. Nielsen has applied his extensive experience in high-speed mixed-signal analog circuit design at such companies as Ericsson, Conexant, and Vitesse. His circuit designs include 40 Gbps InP HBTs, clock and data recovery circuits and demultiplexers, limiting amplifiers, and laser drivers. Dr. Nielsen has also designed a variety of 10.7 Gbps 0.13 μ m CMOS circuits, including output drivers and VCOs. In 12.5 Gb/s SiGe BiCMOS, he has designed CML cell libraries, including output drivers and VCOs, limiting amplifiers, multiphase LC-VCO, and 16:1 multiplexers. Dr. Nielsen received his Ph.D. from the Technical University of Denmark, where he wrote a thesis entitled “Multi-Gigabit ASIC Design” focused on demonstrating 10 Gbps clock and data recovery circuits in standard silicon bipolar technology.

Presenter Biographies (con't.)

Dr. Paul van der Wagt, Principal Design Engineer. Dr. van der Wagt has 15 years of experience in high-speed IC design and device modeling. At Inphi, he has developed high-speed logic ICs with clock rates up to 50 Gbps. Previously, he was a senior scientist at Rockwell Scientific, where he designed world-record bandwidth track-and-hold circuits for commercial use. From 1995 to 1998, Dr. van der Wagt designed and fabricated quantum device circuits for ultra high speed analog-to-digital converters and low-power memory at Texas Instruments Central Research Labs. He holds 12 patents, has authored or coauthored more than 30 papers, and is a senior member of the IEEE. Dr. van der Wagt holds M.S. and Ph.D. degrees in Applied Physics from Stanford University in addition to two M.S. degrees from Twente University, The Netherlands.

