Link Performance Investigation of Industry First 100G PAM4 IC Chipset with Real-time DSP for Data Center Connectivity

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Abstract: We experimentally demonstrate, for the first time by employing newly developed PAM4 chipset and direct detection with commercial 25Gbaud devices, the link operates error free under KR4 FEC threshold at 1310nm wavelength(s) for 100Gb/s up to 40km distance of standard single mode fiber.

OCIS codes: (060.4510) Optical communications; (060.4080) Modulation; (250.3140) Integrated optoelectronic circuits

1. Introduction

It's obvious that the demand for bandwidth will continue to rise rapidly in the data center and server sector. Just recently after years' long industrial debate, the IEEE 400GbE P802.3bs Task Force [1] has adopted optical four level Pulse Amplitude Modulation or PAM4 signaling as the only viable technology standard of data center interconnect for 2km and above distances as well as for low end of 500m and below. Current 100G data center solutions use either four fibers or four wavelengths at 25Gbps per wavelength. The optics usually take up main part of optical module cost. The optical PAM4 modulation reduces optics counts by doubling the bits per symbol at the same baud rate, and transfers the complexity into CMOS electronics with PAM4 encoding, real-time DSP and FEC technologies, so bandwidth improvement can be achieved at a lower cost as compared to existing NRZ solution.

So far prior measurements of PAM4 optical transmission at 25Gbaud and higher have heavily relied on offline post-processing techniques with the aid of expensive instruments, and some high BER floors around 10^{-5}~10^{-6} have been expected [2-5] due to limited memory sizes of captured waveforms. To implement the PAM4 architecture over transition from NRZ, the key integrated circuit (IC) building blocks, as shown in Fig. 1, include the PAM4 DSP engine incorporating real time DSP processing and FEC as well as high linearity, low power and high speed transimpedance amplifiers (TIA) and drivers.

In this paper, we present the availability of industry first 100G PAM4 IC chipset operating error free under KR4 FEC threshold at ~25Gbaud covering various scenarios from over 2km of single mode fiber: 1) single lambda (1λ) 40Gb/s; 2) dual lambda (2λ) 100Gbps with either PIN or APD devices. Using the realized PAM4 IC platform, we experimentally demonstrate, for the first time, up to 40km transmission is successfully achievable for 100 Gb/s with reference to the state of art high sensitivity APD optical receiver [5].

2. PAM-4 IC Implementation Challenges

The multi-purpose PAM4 PHY chip with real time DSP capability is critical for generating the optical PAM4 signals. A block diagram of the DAC (Digital to Analog Converter) based PAM4 PHY chip is shown in Fig. 1. The PAM4 transmitter leverages transmit (TX) DSP, and DAC which maps the input MSB and LSB (Most & Least Significant Bits) bit streams into the PAM4 symbols. Fig. 2 (a) presents the electrical PAM4 eye directly from the DAC, and (b) subsequent PAM4 optical eye diagram from standard 100GbE-LR4 based EML with output power of +2dBm at 1299.8nm (Courtesy of NeoPhotonics).

The DSP engine has the challenging tasks to combat various distortion and noise effects [6] from e.g., bandwidth limiting, intersymbol interference, chromatic dispersion and nonlinear behaviour etc. For receive DSP, the FFE (feed forward equalizer) and DFE (decision feedback equalizer) are considered as two equalizer options for 25Gbaud PAM4. It normally consist of 10-21 taps of FFE and 1-4 taps of DFE. The front ADC and FFE may operate at 1-2 samples per symbol. The FEC (forward error correction) decoder allows the PAM4 decoding at pre-FEC BER values, e.g., better than ~10^{-5}, then the decoded PAM4 digital signal is further enhanced, using standard FEC codes such as KR4 or KP4 FEC [1], to yield "error free" signal, i.e., better than 10^{-15} BER.

For the DSP to be self-adaptive at real time, the tap weights, for both the FFE and DFE, are updated automatically by an adaptive algorithm, and usually implemented using well established least-mean-squared (LMS) algorithms. This is accomplished by applying a close-loop feedback mechanism together with a means for estimating signal quality, e.g., error signal. When the adaptive algorithm controls the weights of the FFE and DFE, it converges to a minimum BER state, when typically coincident with maximum eye opening.

Another important element of implementing PAM4 is the linear O/E front-end and automatic gain control (AGC)

due to the analog nature of the ADC and equalization process. The linearity of the O/E front-end minimizes any further distortion on top of the impaired signal. As the input power can vary widely, a high amount of dynamic range is required. The AGC is normally integrated into the TIA and support an output signal in the range of 10 to ~400 mVpp/side, and holds the output steady regardless of input signal strength over the entire dynamic range.

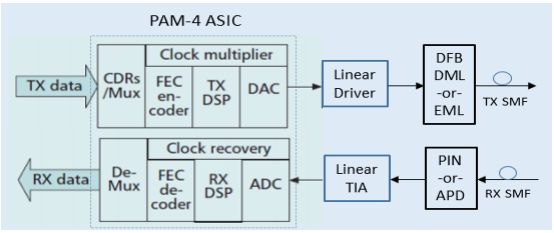

Fig. 1: Typical optical PAM4 transmitter and receiver IC building blocks

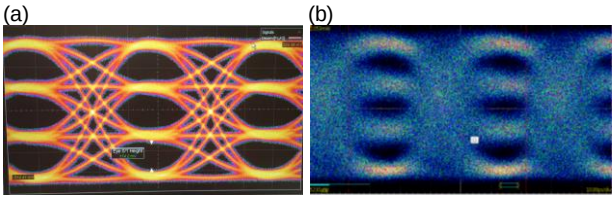

Fig. 2: a) 25Gbuad PAM4 TX electrical eye; b) subsequent PAM4 optical eye diagram from standard 100GbE-LR4 based EML with output power of +2dBm at 1299.8.nm

3. Experimental setups

The experimental PAM4 setups for 1λ×41.25 and 2λ×51.5625 Gb/s systems used in this work are depicted in Fig. 3(a) and (b) running at KR-FEC rates of 20.625GBaud and 25.78125Gbaud, respectively. The multi-purpose PAM4 PHY chip is the heart of the setup. In both experiments, the embedded PRBS generator and checker inside the chip facilitate the true real time BER tests of the end-to-end optical PAM4 link. If it's not specified, we used PRBS 2^{15}-1 throughout this work.

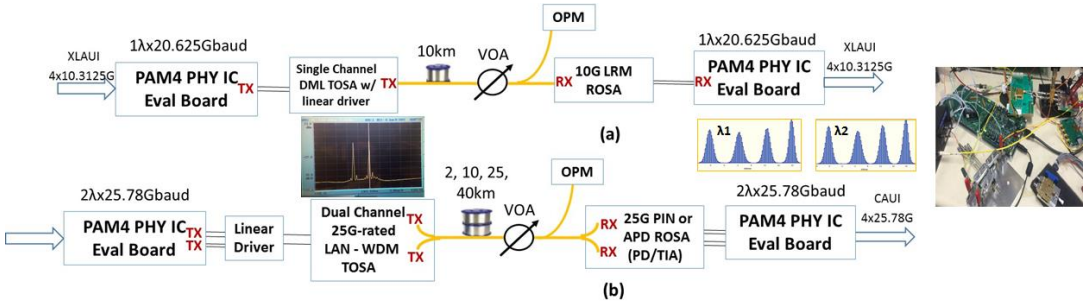

Fig. 3: PAM4 test setup at (a) 1λ 40Gb/s DML, (b) 2λ 100Gb/s EMLs, with RX DSP recovered histograms shown in inset

In the 1λ×41.25Gb/s PAM4 test, one 41.25 Gb/s PAM4 signal was generated differentially at 500 mVpp/side from PAM4 PHY transmit (TX) output. A 1299nm DML with integrated linear Shunt driver was used as optical source [7] (Courtesy of SEDI). One 10-km SMF spool (with an optical loss of 5.6dB) was inserted before VOA (variable optical attenuator) for varying the input power to the optical receiver. For lower cost consideration, a 10G LRM ROSA of 8GHz 3-dB bandwidth (Courtesy of Oplink) was chosen for optical-to-electrical conversion in front of PAM4 PHY receiver (RX).

The 2λ×51.5625Gb/s experimental setup is similar to that of 1λ PAM4 (Fig. 3), but with two wavelengths each running simultaneously at 51.5625Gb/s. The linear driver (IN3214SZ) was fed with differential input and generated single-ended output for driving EML. The two wavelengths at 1299nm and 1304nm from commercial quad EML TOSA module (Courtesy of NeoPhotonics, Avago) were then combined via a LAN-WDM multiplexer and attenuated through VOA, which controlled the input power to the ROSA. Several SMF spools of various distances of 2, 10, 25, 40-km (with optical losses of 1.8, 5.6, 8.7, 13.6dB, respectively) are then inserted for transmission link test. We investigated two kinds of different commercial ROSAs with either PIN (IN3250TA) or APD (IN2860TA). The optical power of each wavelength was controlled and calibrated by VOA and wavemeter before it feeds into the ROSA and was demultiplexed. The insertion losses of LAN-WDM multiplexer, demultiplexer, and VOA are 1.6, 1.5, and 2.6dB, respectively.

4. 1λ 40G 10km transmission

The measured BER curves versus (vs.) receiver (RX) optical power at 20.625Gbaud for back-to-back (B2B) and 10km are presented in Fig. 4. The 1299nm DML is biased at DC current of ~80mA with optical output power of +4.6dBm. The extinction ratio (ER) was around 4.8dB. The power penalty at pre-FEC BER threshold 2.4×10^{-4} for 10km is negligible as compared to B2B case, while the BER floors at BER values of ~1 order of magnitude higher.

This could be understandable, as there exist large bandwidth gap required for the operating baud rate from the 10G LRM ROSA. When the FEC is enabled, the link ran error free with 10km at sensitivity below -9.5dBm.

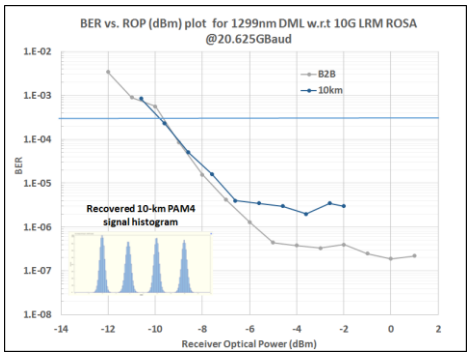

Fig. 4: 40Gb/s PAM4 BER vs. RX optical power over 10km SMF running at 20.625GBaud

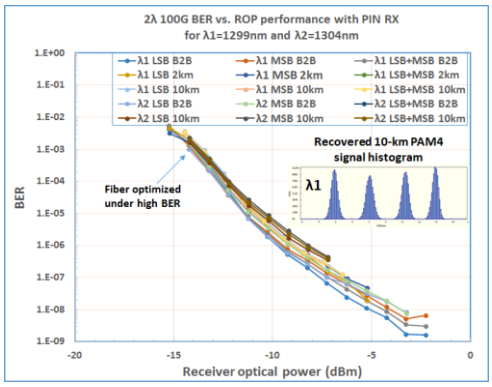

Fig. 5: 2λ×50G PAM4 transmission results with PIN RX

5. 2λ 100G 10km and 40km transmissions

Fig. 5 shows the BER curves with PIN receiver for LSB, MSB and combined (LSB+MSB) bit streams after various distances and with B2B. Both EMLs for λ1 and λ2 are biased at 80mA and maintained at 42ºC. The extinction ratios were around 6.8dB, and 6.5dB, respectively. A slightly worse performance in MSB was observed due to high error probability on the symbol. The Rx sensitivity was around -12.9dBm, while power penalty for 10km fell within 0.5dB than B2B at 2.4×10^{-4} pre-FEC threshold.

The experimental results of 2λ×51.5625Gb/s over 40km are shown in Fig. 6 for λ1 and λ2 respectively. Similarly, the BER for LSB, MSB and combined LSB+MSB are monitored for both wavelengths. Both EMLs for λ1 and λ2 are biased at 100mA and maintained at 42ºC for slightly higher power of over +2dBm. The extinction ratio are around 7.2dB, and 7.0dB, respectively after the negative biasing voltage to the EMLs was optimized. The APD voltage was biased at ~25Vdc. APD shows more than ~6.5dB better sensitivity in B2B than PIN. Around ~1dB penalty was observed between B2B and 40km. The PAM4 signal histograms for 40km were shown in inset indicating both λ1 and λ2 running robustly. When the FEC is enabled, the link ran error free for 40km with margin.

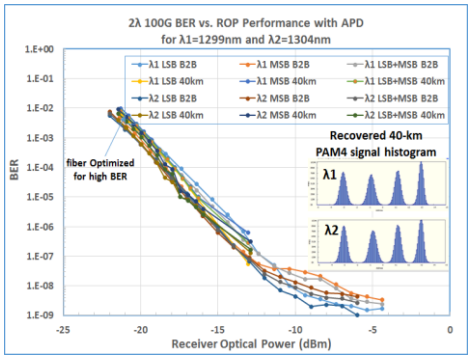

Fig. 6: 2λ×51.5625Gb/s PAM4 BER vs. RX optical power plots with APD for 40km SMF transmission at λ1= 1299nm and λ2=1304nm

6. Conclusions

By leveraging newly developed PAM4 IC chipset, the link performance with real-time DSP in miniaturized silicon format were extensively studied for distance of standard single mode fiber from 2km and above, and it showed error free transmission with great margin under KR4 FEC threshold at 1310nm wavelengths for up to 40km distance. This is the first time to report the 40-km optical transmission with the availability of complete IC platform for enabling small form factor modules such as CFP4 and QSFP28 [8].

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