60 GHz Bandwidth InP HBT Transimpedance Amplifiers for Optical Link Applications

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***Abstract* — A set of transimpedance amplifiers with the bandwidth in the 55 – 65 GHz range for applications in the long haul optical networks is presented. Transimpedance value is in the 250 to 300 Ω range, integrated input noise current ≈ 7.5 – 8.5 μA (0 – 60 GHz) and the output amplitude is between 600 mV_{pp} and 900 mV_{pp} (single ended) – dependent on the version. The circuits are designed in the InP HBT technology and consume 220 to 350 mW with +3.3 V supply voltage. The circuits are currently being fabricated at the GCS foundry and the test results and mask photos will be presented in the Conference paper.**

I. Introduction

The development of components for broadband data transmission has been one of the diving forces in the semiconductor industry. With the 10 Gb/s systems fairly well established in the market the next step is to switch to higher data rates in the 40 – 50 Gb/s range and possibly to 80 – 100 Gb/s (NRZ) in the near future [1]. This paper presents the design of the input component of the optical link receiver: the transimpedance amplifier (TIA) for 50 Gb/s RZ of >100 Gb/s NRZ transmission. Primary application of this TIA is to be in the long haul optical networks using optical amplifiers. Therefore relatively low electrical gain - 250 Ω - and high maximum input current from the photodiode – 4 mA – have been specified. Similar circuits in InP HEMT technology with 50 GHz bandwidth have recently been presented [2]. Several versions of the TIA have been designed, differentiated by the output drive capabilities, photodiode connection, and by the details in particular stages to optimize performance. The design is based on the InP HBT technology developed by the Global Communication Semiconductors, Inc. (GCS) with transistor f_T and f_{max} exceeding 150 GHz.

II. Design Issues and Constraints

The structure of the chips (Fig. 1) follows the typical arrangement. Input transimpedance stage is responsible for noise properties of the chip and should provide most of the gain. Single ended to differential converter should accept the full ITIA output signal swing and convert it to balanced outputs with good common mode rejection.

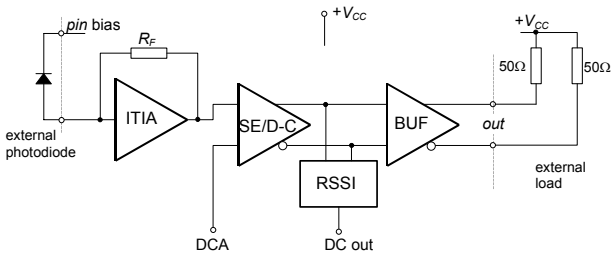


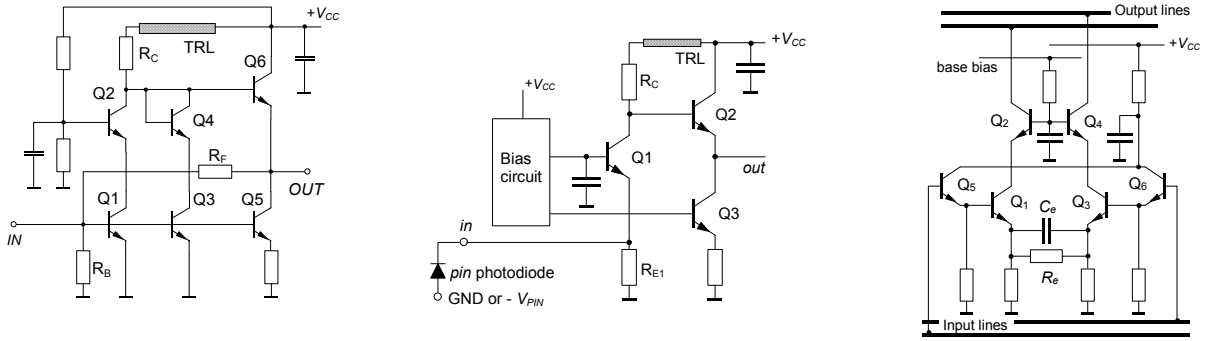
Fig. 9. Block diagram of the TIA chip. *ITIA* – input transimpedance stage, *SE/D-C* – single ended to differential signal converter, *RSSI* – received signal strength indicator, *BUF* – output buffer amplifier, *DCA* – output DC balance adjustment

Output buffer stage should supply enough current to the external 50 Ω loads to assure specified output amplitude – 600 mV_{pp} or 900 mV_{pp} in this case. This stage also provides moderate amount of signal limiting at maximum input current (4 mA) and should not degrade the performance of the system under these conditions.

Several factors restrict available optimization approaches to the design. The use of the indium phosphide HBT technology excludes *PNP* transistors, which would facilitate the use of dynamic loads in amplifier stages (high DC gain) and level shifting. High maximum input current value and the absence of dynamic loads cause large variations in the input transistor collector current and hence significant change of its properties vs. signal level. Analytic approach to circuit optimization is of limited value and experimental design based on nonlinear simulation must be used. Certain circuit parameters (feedback resistor R_F, bias currents) are determined by the overall specifications and little room is left for adjustments. The design is generally aimed at the best transient performance (eye diagrams), which may conflict with the noise parameter improvement.

III. Input Stage Design

Two typical solutions used for the input stage are shown in Fig. 2. Circuit a) is intended for photodiodes with the anode output and positive diode bias voltage while circuit



a) input stage for positive input current b) input stage for negative input current c) elementary cell of the output buffer

Fig. 2. Simplified circuit diagrams for components of the transimpedance amplifier. *TRL* – a section of transmission line

b) operates best with cathode output (and negative bias) diodes. Design was optimized for minimum noise within the limits imposed by the signal handling capability. Transimpedance of both circuits is about 180 Ω.

Circuit a) is built as a simple transimpedance stage with emitter follower (Q6) feedback [3]. Voltage gain stage (Q1,Q3) is split into two parts: Q1-Q2 forming a cascode to minimize input capacitance, while Q3-Q4 form a CE amplifier. Such configuration helps to control the phase shift in the feedback loop with relatively low R_F values. Full cascode configuration introduces too much phase shift and results in excess gain in the 20 – 40 GHz range.. Transistor Q5 provides certain amount of feedforward action for fast signal edges, and its C_{bc} junction capacitance – in parallel with R_F – compensates for the phase shift in the feedback loop. Inductive compensation with short sections of narrow transmission lines (TRL) is used in the gain stages. Required L values are in the 80 – 150 pH range.

Circuit b) uses common base configuration with inductive compensation of the collector load. Bias circuit provides low impedance to the base of Q1 down to very low frequencies to assure flat gain and group delay response. The circuit is simple, but the low input impedance makes its response very sensitive to variations in the bonding wire length – see the next section.

The TIA has been designed to connect to the external photodiode chip with bonding wires. The inductance of the bonding wire poses a real challenge in such broadband design. It may be used to extend the bandwidth of the system but the circuit should not be very sensitive to the inevitable variations in the bonding wire length.

Simple model of the diode-TIA interface is shown in Fig. 3. The current transfer ratio $A_{it} = I_{in}/I_d$ for this model is given by (1). The generally low-pass function may have

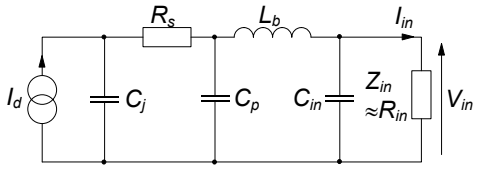


Fig. 3. Model of the TIA input circuit including the photodiode. C_j – diode junction capacitance, R_s – diode series resistance, C_p – contact pad capacitance, L_b bonding wire inductance, C_{in} – input TIA chip capacitance – mostly bonding pad, Z_{in} – input stage input impedance

complex poles dependent on the value of L_b and Z_{in}. For the circuits presented here Z_{in} has relatively small imaginary part (<25% R_{in}) and R_{in} varies no more than 30% across full bandwidth. Subsequently it was assumed that $Z_{in} \approx R_{in} \approx \text{const}(f)$.

$$A_{it}(s) = \frac{I_{in}}{I_d} = \frac{1}{1 + as + bs^2 + cs^3 + ds^4}$$

where

$$\begin{aligned} a &= R_{in}(C_j + C_p + C_{in}) + R_s C_j \\ b &= L_b(C_j + C_p) + R_s C_j R_{in}(C_{in} + C_p) \\ c &= L_b\left[C_{in} R_{in}(C_p + C_j) + C_p C_j R_s\right] \\ d &= L_b C_p R_s C_j R_{in} C_{in} \end{aligned} \qquad (1)$$

Moderate gain peaking in the input stage is advantageous to compensate for the loss of gain in the following stages. Here it was arbitrarily assumed that 3 dB of gain increase at 60 GHz is a good solution. The required L_b in this case may be computed from (1). Fig. 4 shows the variation in gain at f = 60 GHz vs. L_b computed for representative data: C_j = 30 fF, R_s = 20 Ω, C_p = 20 fF, C_{in} = 15 fF. Sensitivity to L_b variations may be evaluated from this figure as well.

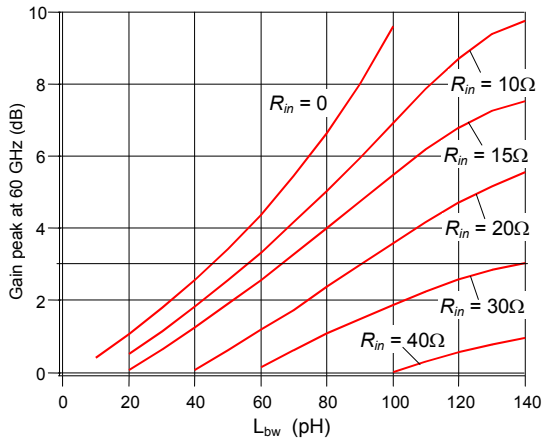


Fig. 4. Gain peaking at f = 60 GHz vs. L_{bw} for various input resistances R_{in}

It must be noted that usually L_b includes the contribution from two bondings to the diode chip and practical minimal value of L_b is on the order of 100 pH. Thus there is no reason to design the TIA for the lowest possible R_{in} if the bonding wire connection is planned. The upper limit of R_{in} is dictated by the resulting bandwidth. For the data used above that limit is ≈ 37 Ω - if the frequency of the maximum gain (the peak) should not be lower than 60 GHz.

The amount of peaking that may be used at the input is also limited by the allowable group delay variation. The group delay of the transfer function (1) is shown in Fig. 5. Large changes in τ_g occurring above 60 GHz are not very critical (10Ω and 15Ω case) but the peaks occurring in the 30 – 60 GHz range tend to add to similar peaks from the stages following.

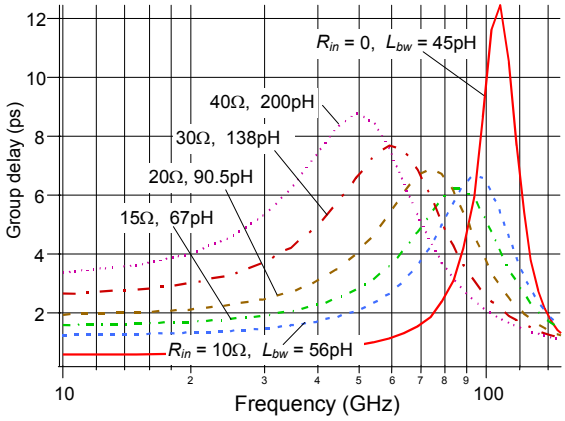


Fig. 5. Group delay vs. frequency for bonding wire inductance selected for 3 dB gain peaking at 60 GHz

The noise performance of the TIA is determined mostly by transistors used and there are limited options for improvement with certain components fixed by other requirements. Input referred noise would be improved with higher L_b values that are needed for acceptable transient response. Typical noise contribution from various components for the circuit a) in Fig. 2 is shown below.

Q3 – 27.4%	R_C – 2.0 %
Q1 – 15.1 %	Q2 – 1.2 %
R_B – 7.0 %	Q4 – 0.4 %
R_F – 3.5 %	Q5 – 0.3 %
Q6 – 3.1 %	

The numbers indicate the portion of the total output noise power integrated in the 0.01 – 60 GHz bandwidth attributed to each component. There is very little increase (≈ 4%) in noise power beyond the 60 GHz limit.

To decrese the base resistance the emitter widths were maximized within the constraints imposed by bandwidth requirements. Total emitter width of the Q1,Q3 pair is in the 10 – 12 μm range.

IV. Output Stage and General Design Approach

Output buffer contains a number of cells shown in Fig. 2c connected in parallel. The version for 600 mV output amplitude contains three cells with 1x5 μm transistors, while higher amplitude versions are built either with 5 such cells or with 2 and 3 cells with 1x10 μm transistors.

The cascode configuration was chosen for the the largest bandwidth with good linearity and high output impedance, which helps to maintain low reflections at the output ($|S_{22}|$ < -10 dB to >60 GHz). Moderate amount of gain compensation was used in the differential stage with C_e capacitor, which was kept as small as possible to avoid adverse affects the group delay of the amplifier. Basic cells in the output buffer are separated by sections of transmission lines thus forming a structure similar to a distributed amplifier. The number of cells is too small to exploit full benefits of the distributed amplification, but appropriate selection of line lengths improves the bandwidth by 10 to 15 %.

Extremely broadband circuits like the TIAs presented here require very careful consideration of design details. Certain portions of chips were modeled with the electromagnetic simulator to account properly for discontinuities and transmission line properties. Based on these simulations models have been created for the Cadence® software, which was used for design. Particular attention was paid to the bias distribution and decoupling network. It was necessary to introduce small damping resistors in series with many blocking capacitors to decrease ringing and group delay deviation. Some distortions introduced by the V_{CC} bias network still may be seen in Fig. 6 in the 1– 2 GHz frequency range.

V. Parameters of Transimpedance Amplifiers

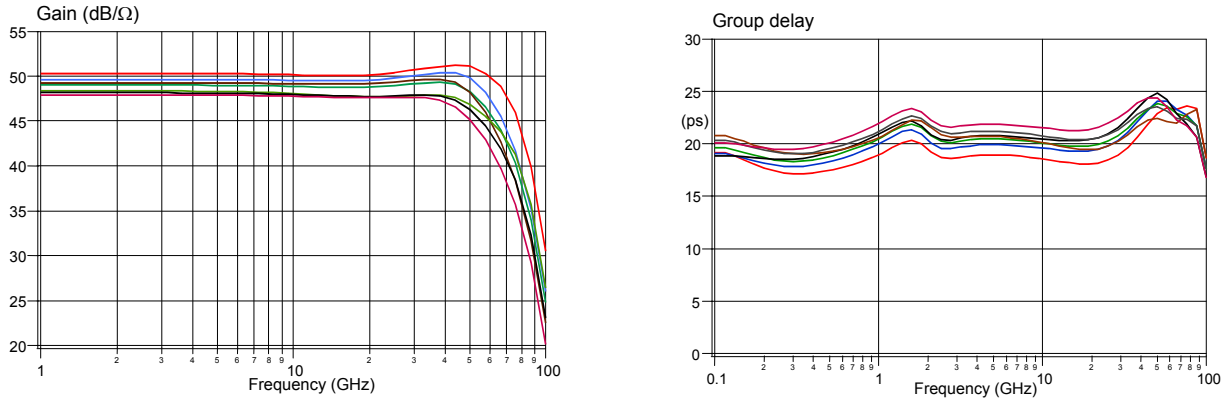


Fig. 6. Simulated gain and group delay for -10° C ÷ +100° C operating temperature range and supply voltage changes in the 3.1V ÷ 3.5 V range. 600 mV output amplitude version

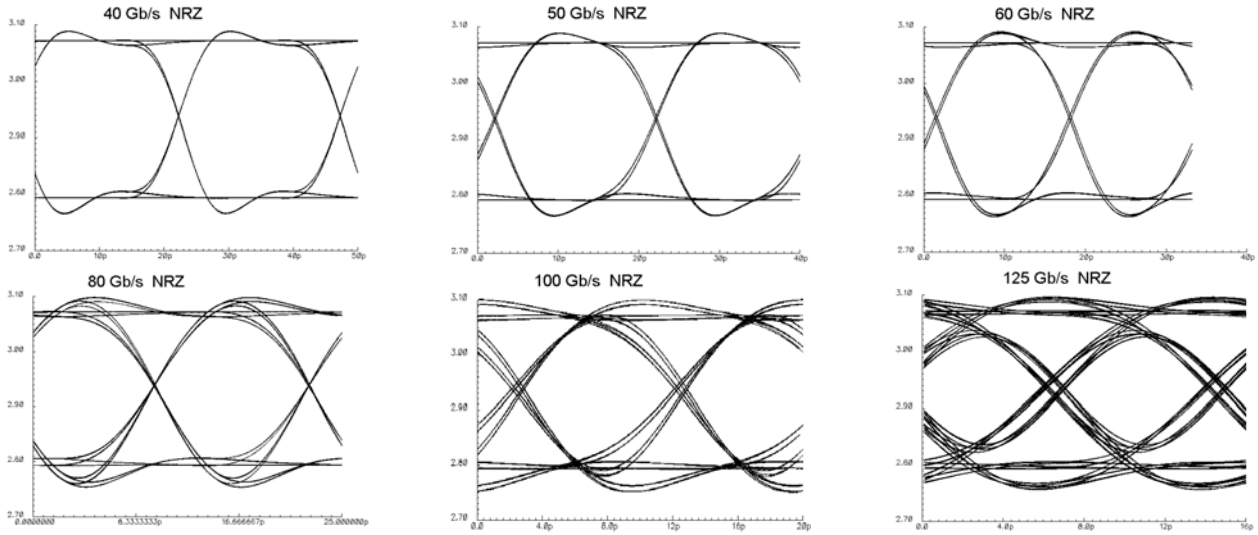


Fig. 7. Simulated eye diagrams for various bit rates (NRZ format) at an input current amplitude of 1 mA

The bandwidth at T = 50°C and V_{CC} = 3.3 is about 60 – 65 GHz for versions with smaller number of cells in the output buffer. 5 cell version exhibits about 55 GHz simulated bandwidth. Selected simulation results are shown in Fig. 6 and 7. High ambient temperatures (85 - 100°C) degrade the bandwidth by about 10 – 12 %. Input current noise integrated over 0.01 – 60 GHz bandwidth is 7.5 μA for the version with a simple (one differential amplifier) single ended to differential converter and 8.5 μA for a more complicated SE/D-C stage.

References

[1] T.Li, "Crouching technologies and hidden profits: perspectives and prospects of optical networks.", *NFOEC 2001 – 17th Annual Conf. Workshop notes.*, July 2001.

[2] H. Shigematsu et al. " A 49-GHz preamplifier with a transimpedance gain of 52 dBΩ using InP HEMTS", *IEEE J. Solid-State Circuits*, vol. 36, no. 9, pp. 1309-1313, Sept. 2001.

[3] K. Ohhata, T. Masuda, E. Ohue, K. Vashio, "Design of a 32.7-GHZ bandwidth AGC amplifier IC with wide dynamic range implemented in SiGe HBT," *IEEE J. Solid-State Circuits*, vol. 34, no. 8 pp. 1290-1297, Sept. 1999.